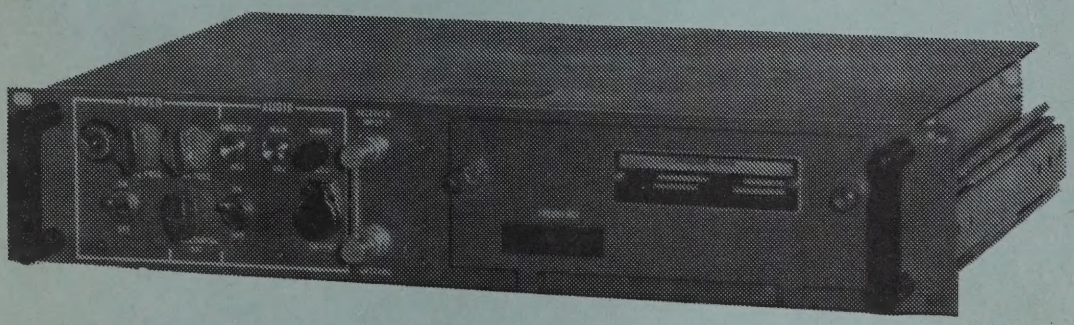
Service And Circuit Diagrams Manual

GRR 21,22 23 24 ITT 3101, 3102

VHF/UHF RECEIVER

116—149.975 MHz Model No. 3101 • 225—399.95 MHz Model No. 3102



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INTRODUCTION

This manual contains information to install, operate, and maintain the VHF Receiver Model No. 3101 and the UHF Receiver, Model No. 3102.

Both Receivers, Model No. 3101 (VHF) and Model No. 3102 (UHF), are identical in physical size and are designed for mounting in a standard 19-inch rack or cabinet.

VHF Receiver Model No. 3101 operates in the amplitude modulation (AM) mode. It is capable of receiving on any one of 680 channels spaced 50 kHz apart or on any one of 1360 channels spaced 25 kHz apart between 116.00 mHz and 149.95 mHz (VHF). By exchanging certain of the frequency determining modules with their corresponding UHF modules, the Model No. 3102 configuration is established which provides receiving capability on any one of 3500 channels spaced 50 kHz apart or on any one of 7000 channels spaced 25 kHz apart between 225.00 mHz and 399.95 mHz (UHF).

Information in this manual is presented in six chapters. Chapter 1 contains a description of the equipment from a functional standpoint including its capabilities and limitations. Information is provided covering leading particulars, equipment supplied, and auxiliary equipment required but not supplied. Chapter 2 contains information for installation planning, logistics, installation procedures, and preparation for reshipment. Chapter 3 describes all operating controls, indicators, and interlocks, and provides starting, operating, stopping, and emergency operation procedures. Chapter 4 discusses the principles of operation on a functional system basis and also to an operational or signal sequence flow. Chapter 5 includes maintenance and alignment procedures. Chapter 6 contains circuit diagrams.

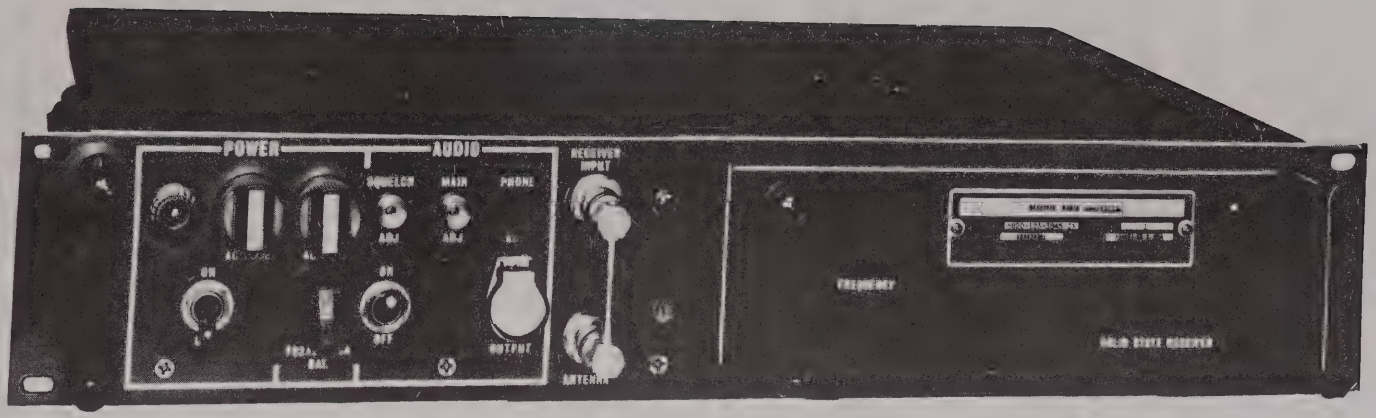


Figure 1-1. Receivers, Model No. 3101 (VHF) and Model No. 3102 (UHF).

CHAPTER 1

GENERAL INFORMATION

1-1. INTRODUCTION. This chapter contains information concerning VHF Receiver Model No. 3101 and UHF Receiver Model No. 3102. A description of the equipment, its purpose and strategic mission, capabilities and limitations, leading particulars, and operation are discussed in the following paragraphs.

1-2. DESCRIPTION AND PURPOSE.

1.3. The VHF Receiver Model No. 3101, hereinafter referred to as the VHF receiver, is a single channel solid-state superheterodyne receiver that operates in the amplitude modulation (AM) mode in the radio frequency (rf) range of 116.00 to 149.95 MHz. It is capable of reception in this frequency range on any one of 680 channels spaced 50 kHz apart using the 50 kHz IF crystal filter or on any one of 1360 channels spaced 25 kHz apart using the 25 kHz IF crystal filter. The operating frequency is determined by either the oscillator crystal frequency selected or the dial setting of the oscillator-synthesizer.

1.4. The UHF Receiver Model No. 3102, hereinafter referred to as the UHF receiver, is a single channel solid state superheterodyne receiver that operates in the amplitude modulation (AM) mode in the radio frequency (rf) range of 225.00 to 399.95 MHz. It is capable of reception in this frequency range on any one of 3500 channels spaced 50 kHz apart using the 50 kHz IF crystal filter or on any one of 7000 channels spaced 25 kHz apart using the 25 kHz IF crystal filter. The operating frequency is determined by either the oscillator crystal frequency selected or the dial setting of the oscillator-synthesizer.

1-5. An oscillator-synthesizer module is available which is directly interchangeable with and replaces the crystal oscillator module.

1-6. The VHF receiver, when equipped with the oscillator-synthesizer, has the potential capability of reception on any one of 2720 channels spaced 12.5 kHz between 116.00 and 149.9875 MHz, providing a narrowband IF crystal filter (not specified at this time) is selected to reduce channel interference.

1-7. The UHF receiver, when equipped with the oscillator-synthesizer, is capable of reception on any one of 7000 channels spaced 25 kHz between 225.00 and 399.975 MHz.

1-8. Frequency selection using the oscillator-synthesizer module is obtained by setting its front panel switches to the required input frequency to the mixer-multiplier module.

1-9. An oscillator-multiplier module is available which is directly interchangeable with the crystal-oscillator module or the oscillator-synthesizer module. This oscillator-multiplier module differs from the crystal oscillator series in that it uses a fundamental crystal rather than a fifth overtone type and the crystal oven is eliminated. Frequency accuracy is determined by "pulling" the crystal. Tuning is accomplished to the exact frequency by monitoring the frequency with a frequency counter.

1-10. The VHF receiver and the UHF receiver are designated for world-wide deployment in the air-traffic control service and provide air-to-ground and point-to-point communications. See Figure 1-1.

1-11. The VHF receiver and the UHF receiver are designed to perform reliably in an air-traffic control environment.

1-12. The VHF receiver and the UHF receiver are self-contained assemblies, each with its own integral power supply.

1-13. The VHF receiver and the UHF receiver have provision for use of an external precision oscillator in lieu of a crystal for frequency control.

1-14. The VHF receiver is designed with the capability to operate two receivers in parallel on a single antenna tuned to channels separated by a minimum of 1 MHz.

1-15. The UHF receiver is designed with the capability to operate two receivers in parallel on a single antenna tuned to channels separated by a minimum of 3 MHz.

1-16. LEADING PARTICULARS.

1-17. The physical and electrical characteristics of the VHF receiver and the UHF receiver are listed in Table 1-1.

1-18. CAPABILITIES AND LIMITATIONS.

1-19. The capabilities and limitations of the VHF receiver and the UHF receiver are listed in Table 1-2.

1-20. EQUIPMENT SUPPLIED.

1-21. Equipment supplied comprising the VHF receiver and the UHF receiver is listed in Table 1-3.

1-22. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

1-23. Tools and test equipment required for maintenance but not supplied with the VHF receiver and the UHF receiver are listed in Table 1-4.

Table 1-1. Leading Particulars

CHARACTERISTIC	REQUIREMENT
PRIMARY INPUT POWER	105, 120, 210, or 240 volts ± 10%, single phase 47 hz to 420 hz, 50 watts maximum. If ac power fails, 24-volt lead acid battery (not supplied with the equipment) is automatically switched in to provide emergency power for a period dependent on the battery ampere-hour capacity. A 100-ampere-hour battery will provide for approximately 120 hours for one receiver.
PHYSICAL DESCRIPTION	
Dimensions	3-1/2 inches high; 19 inches wide; 12-1/4 inches deep (Standard 19-inch rack or cabinet mounting).
Weight	22 pounds
CABLE REQUIREMENTS	Provided by Air Traffic Control Central
ENVIRONMENTAL	
Operating	Ambient Temperature: $-29^{o}C$ to $+60^{o}C$ Relative Humidity: 5% to 95% (± 5%) AC Line Voltage: 105v ± 10%, 120v ± 10%; 210v ± 10%; 240v ± 10% AC Line Frequency: 47 hz to 420 hz DC: 22 to 30 volts Duty Cycle: Continuous unattended Altitude: 0 to 10,000 ft. MSL Warm-up Time: 30 minutes maximum with crystal oscillator module; 5 minutes maximum with oscillator-synthesizer module. Intermediate Frequency: 20.6 mhz Crystals: Nonstandard type, not supplied with equipment. Stability to achieve frequency accuracy of ± 0.001% when qualified to MIL-C-3098 using procedures of MIL-STD-683. Frequency Accuracy (Oscillator-Synthesizer) ± 0.0005% after 5 minute warm-up.
Non-operating and Storage	Ambient Temperature: $-62^{o}C$ to $+71^{o}C$ Relative Humidity: 5% to 95% Barometric Pressure: 3.34 inches Hg to 31 inches Hg

Table 1-2. Capabilities and Limitations

CHARACTERISTIC	REQUIREMENTS
VHF RECEIVER	
Frequency Range (Oscillator and Oscillator-Multiplier Module	116.00 to 149.95 MHz with 680 channels spaced 50 kHz within this range or 1360 channels spaced 25 kHz.
Frequency Range (Oscillator-Synthesizer Module)	116.00 to 149.9875 MHz with 2720 channels spaced 12.5 kHz within this range in addition to those listed above.
UHF RECEIVER	
Frequency Range Oscillator and Oscillator-Multiplier Module	225.00 to 399.95 MHz with 3500 channels spaced 50 kHz within this range or 7000 channels spaced 25 kHz.
Frequency Range (Oscillator-Synthesizer Module)	225.00 to 399.975 MHz with 3500 channels spaced 50 kHz within this range or 7000 channels spaced 25 kHz.
VHF/UHF RECEIVER	
Frequency Accuracy	Crystal controlled; semiconductor proportionally controlled crystal oven. No more than ± 0.001% drift from operating frequency after 30-minute warm-up. Oscillator synthesizer; no more than ± 0.0005% drift from operating frequency after 30-minute warm-up.
Sensitivity	With a 3.0 μv signal (VHF and UHF) 30% ± 5% modulated at 1 kHz applied to antenna input from a 50-ohm source, and output of 100 milliwatts into a 600-ohm load with a 10 dB (minimum) signal-plus-noise-to-noise ratio is obtained.
Selectivity for 50 kHz Channel Spacing (Oscillator-Synthesizer)	IF Bandwidth Attenuation — VHF — UHF 6 dB — ± 18 kHz Min. — ± 18 kHz Min. 20 dB — ± 27 kHz Max. — ± 27 kHz Max. 40 dB — ± 31 kHz Max. — ± 31 kHz Max. 60 dB — ± 35 kHz Max. — ± 35 kHz Max.* 80 dB — ±100 kHz Max. — ±200 kHz Max.** * Up to 350 MHz, ± 40 kHz for frequencies > 350 MHz. **Up to 350 MHz, ± 275 kHz for frequencies > 350 MHz.
Selectivity for 25 kHz Channel Spacing (Oscillator Synthesizer)	IF Bandwidth Attenuation — VHF — UHF 6 dB — ± 10 kHz Min. — ± 10 kHz Min. 20 dB — ± 17 kHz Max. — ± 17 kHz Max. 40 dB — ± 21 kHz Max. — ± 21 kHz Max. 60 dB — ± 27 kHz Max. — ± 27 kHz Max.* 80 dB — ±100 kHz Max. — ±200 kHz Max.** * Up to 350 MHz, ± 30 kHz for frequencies > 350 MHz **Up to 350 MHz, ± 275 kHz for frequencies > 350 MHz

Table 1-2. Capabilities and Limitations (Cont.)

CHARACTERISTIC	REQUIREMENT	
Selectivity (50 kHz Channel Spacing) (Oscillator Module or Oscillator-Multiplier Module)	Attenuation 6 dB 80 dB	Bandwidth ±18 kHz minimum ±18 kHz maximum
Selectivity (25 kHz Channel Spacing) (Oscillator Module or Oscillator-Multiplier Module)	Attenuation 6 dB 20 dB 40 dB 60 dB 80 dB	Bandwidth ±10 kHz minimum ±17 kHz maximum ±19 kHz maximum ±22 kHz maximum ±25 kHz maximum
IF Output	With 3.0 µV signal 30% modulated produces a nominal output of 125 mV ac.	
Audio Output	Two unbalanced ungrounded transformer outputs. Each 100 milliwatts into 600-ohm resistive load.	
Audio Frequency Response	Not more than +1 dB or -2 dB from 300 Hz to 3000 Hz.	
Automatic Gain Control	Receiver output shall not vary more than 3 dB as a 6 µV input signal modulated 30% ± 5% is increased to 1 volt.	
Automatic Gain Control Time Constant	100 millisecond attack; 100 millisecond decay maximum.	
Squelch	Receiver output muted pending carrier application of not greater than 3.0 µV with squelch sensitivity at maximum setting and not less than 50 µV with squelch sensitivity at minimum setting.	
Noise Limiter (When receiver contains noise limiter module.)	For use in installations where radar pulse interference is high; replaces buffer amplifier module.	
Buffer Amplifier (When receiver contains buffer amplifier module.)	Provides impedance matching and isolation of the crystal filter (FL-1) from the mixer multiplier (A2).	

Table 1-3. Equipment Supplied

OFFICIAL NOMENCLATURE	COMMON NAME
VHF Receiver Model No. 3101	VHF Receiver
UHF Receiver Model No. 3102	UHF Receiver
Interface Cable Kit P/N 8006148G1 (Consist of) Cable (W1)* Special Purpose, P/N 8006147G1 Connector, Plug, Elect. P/N 3108A-18-8S Clamp, Cable P/N MS3057-10A	
Noise Limiter or Buffer Amplifier (Optional Equipment)	

* Approx. six feet long with ac power line connector UP131M.

Table 1-4. Equipment Required But Not Supplied

DESCRIPTION	MODEL OR TYPE DESIGNATOR
Optional Interface Cable Kit	ITT 8006148G1
Plug-In Unit, Electronic	Tektronix, 1A1
Oscillator, Audio	Hewlett Packard 200AB
Oscilloscope	Tektronix 515A
Counter, Frequency Measuring	Hewlett Packard 5245L
Plug-In Unit, Electronic	Hewlett Packard 5253B
Generator, Sweep	Texscan, RS50
Voltmeter	Hewlett Packard 427A
Voltmeter, RF	Boonton, 91CA
Oscilloscope	Tektronix, RM547
Plug-In Unit, Electronic	Tektronix IL20
Plug-In Unit, Electronic	Tektronix, 1S1
Extension Cable Set	ITT 8004810G1
Generator, Signal	Hewlett Packard 608C/D
Meter, Vector Impedance	Hewlett Packard 4815A
Distortion Analyzer	Hewlett Packard 334A
Voltmeter, Electronic	Fluke 801
600 Ohms Impedance Headphones	Telephonics NT 4998A
Crystal Unit, Quartz	CR-143 (Holder Type HC-27/U)

CHAPTER 2

INSTALLATION

2-1. INTRODUCTION. Information and instructions necessary to unpack, install, make operable and prepare the VHF receiver and the UHF receiver for reshipment are included in this chapter. Section I provides installation planning information, Section II covers receipt and unpacking of the equipment. Section III provides installation procedures, and Section IV contains preparation for reshipment data.

SECTION I

INSTALLATION PLANNING

2-2. GENERAL.

2-3. The VHF receiver and the UHF receiver are installed in standard relay racks in the Air Traffic Control Central. See paragraph 2-11 for relay rack cable plug requirements, figure 2-1 for typical relay rack bracket mounting and figure 2-2 for outline dimensional drawing.

2-4. Normally the receivers contain a buffer amplifier module which provides impedance matching and isolation of the crystal filter (FL-1) from the mixer multiplier (A2). In areas of high radar pulse interference a noise limiter module may be substituted for the buffer amplifier module. The noise limiter module effectively blanks the radar pulses.

SECTION II

LOGISTICS

2-6. RECEIVING DATA.

2-7. The VHF receiver and the UHF receiver are packed in separate cleated 3/8-inch plywood boxes. Table 2-1 shows the packed and unpacked dimensions and weights of the receivers. The receivers are packed in snug fitting, expanded polystyrene containers, then completely sealed in a barrier pouch and packed in the plywood box.

Table 2-1. Unpacking Data

QTY	DESCRIPTION	UNPACKED DIMENSIONS	PACKED DIMENSIONS	UNPACKED WEIGHT	PACKED WEIGHT
1	VHF Receiver	3-1/2 in. high; 21 in. wide; 12-1/4 in. deep	9-1/2 in. high; 23 in. wide; 24 in. deep	22 lbs	38 lbs
1	UHF Receiver	3-1/2 in. high; 21 in. wide; 12-1/4 in. deep	9-1/2 in. high; 23 in. wide; 24 in. deep	22 lbs	38 lbs

2-8. UNPACKING DATA.

2-9. Before unpacking the equipment, inspect the shipping containers for evidence of in-transit damage. After the equipment is unpacked, inspect for obvious damage such as bent or broken components, connectors, etc. Check particularly for any obvious damage to the connectors at the rear of the receiver chassis.

2-10. CABLE REQUIREMENTS.

2-11. Cable requirements for the receiver are provided as a part of the Air Traffic Control Central; however, the following specific cable plugs are required to properly install the receiver in the relay rack. if the optional interface cable kit is not available.

Mating plug to J2, MS3108R-18-8S (Preferred)

Mating plug to J2, MS3108A-18-8S (Alternate)

Mating plug to J2, MS3108B-18-8S (Alternate)

Mating plug to J2, MS3106A-18-8S (Alternate)

Mating plug to J2, MS3106B-18-8S (Alternate)

Mating plug to J2, MS3107A-18-8S (Alternate, Quick Disconnect)

Mating plug to J2, MS3107B-18-8S (Alternate, Quick Disconnect)

AC power plug to J1, Hubbell, AC Twist Lock Receptacle, No. 7484

Antenna Input Plug, Type N J13

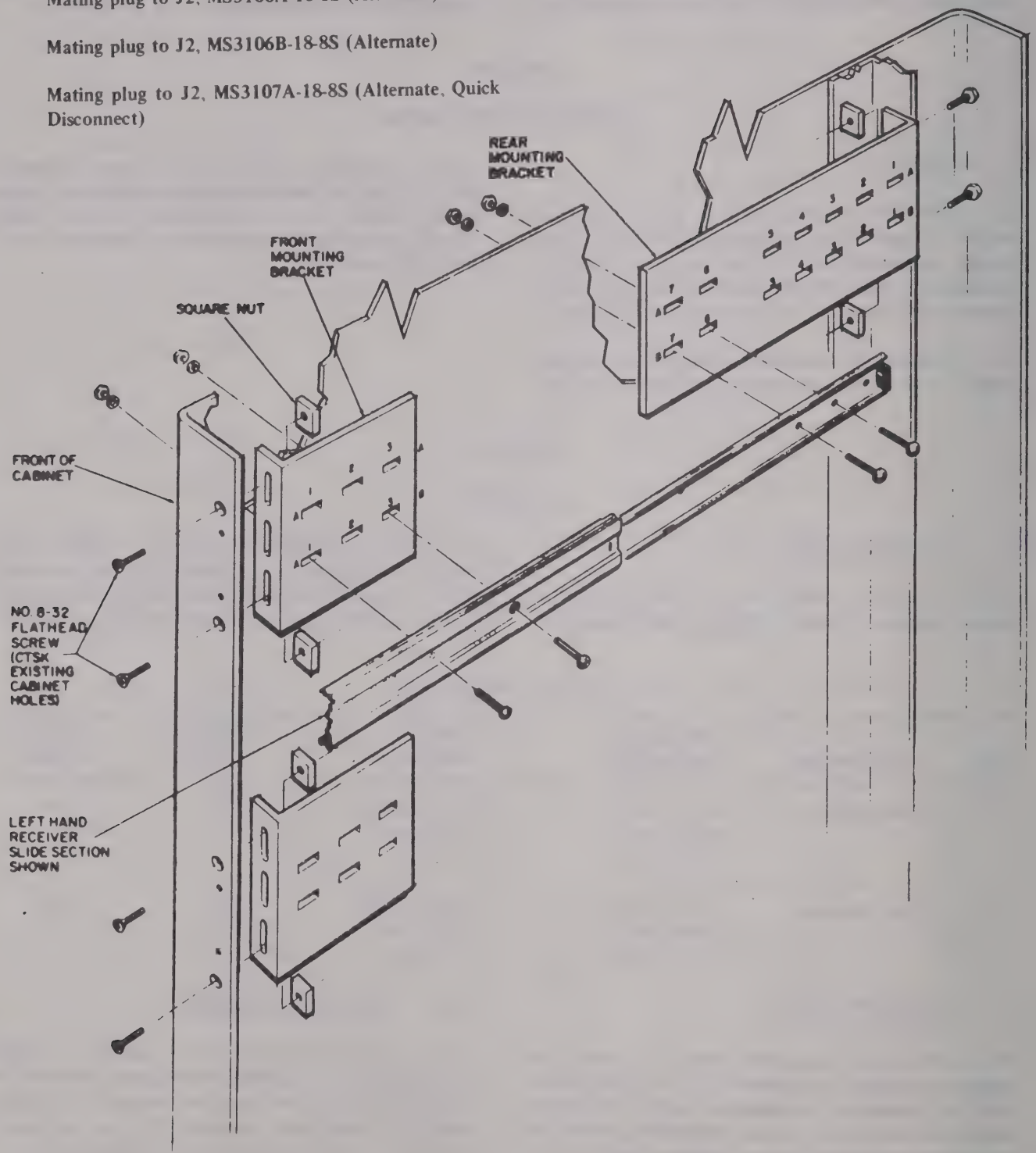

REAR MOUNTING BRACKET
FRONT MOUNTING BRACKET
SQUARE NUT
FRONT OF CABINET
NO. 8-32 FLATHEAD SCREW (CTSK EXISTING CABINET HOLES)
LEFT HAND RECEIVER SLIDE SECTION SHOWN

Figure 2-1. Typical View Relay Rack Mounting Bracket (Left-Side)

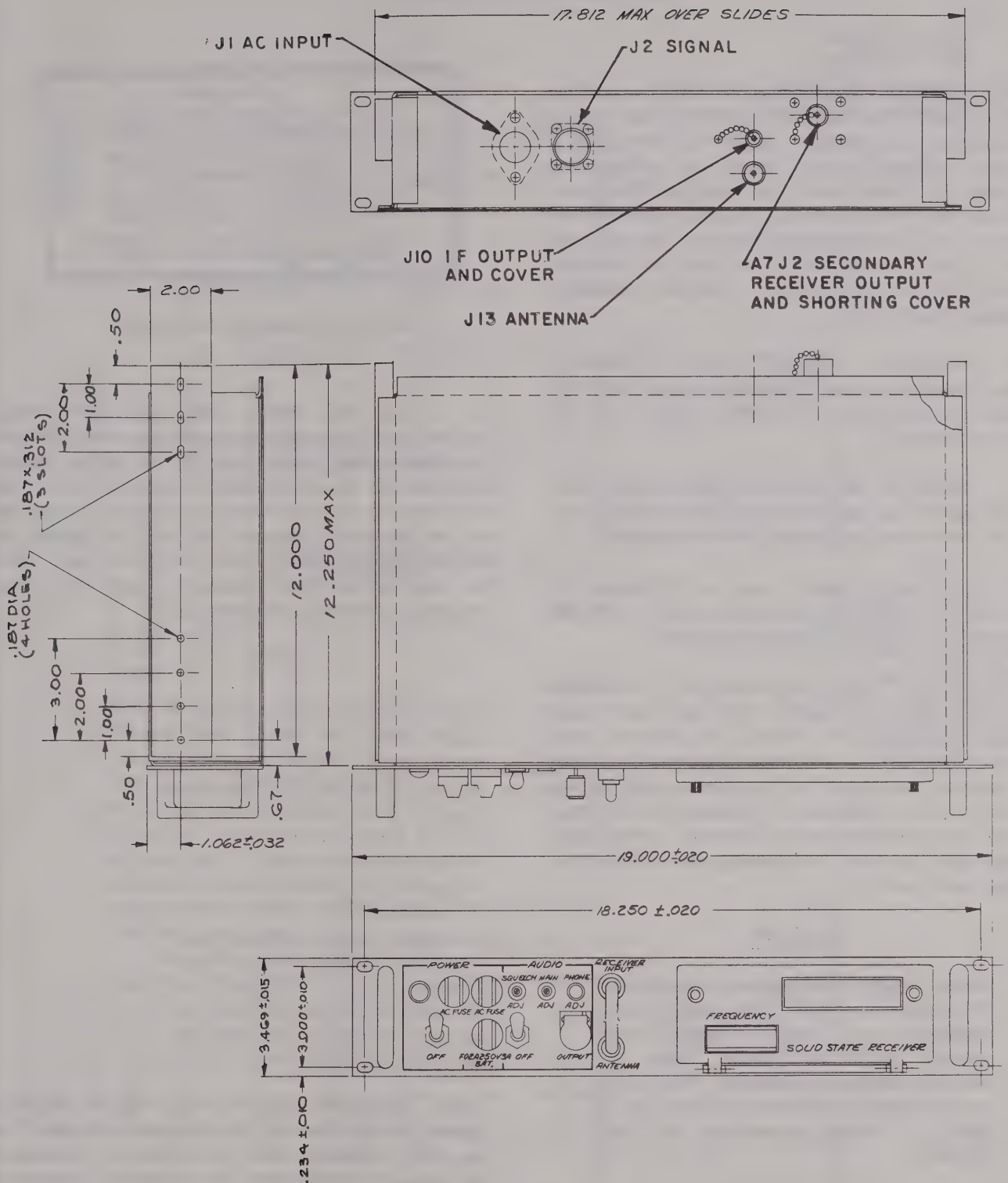


Figure 2-2. Outline Dimensional Drawing

SECTION III

INSTALLATION PROCEDURES

2-12. INSTALLATION.

2-13. The VHF receiver and the UHF receiver are provided with a 3-section slide attached to each side of the chassis. The stationary member of each slide is provided with four 3/16-inch holes at one end and three 3/16-inch by 5/16-inch slots at the other end. These holes and slots are used for attaching the slides with machine screws to the corresponding brackets in the rack. See figure 2-1 for a typical view of the relay rack mounting bracket (left-side). Figure 2-2 is an outline dimensional drawing of the receivers.

2-14. MOUNTING BRACKETS. Figure 2-4 shows an outline drawing of a type A bracket required for CY-597 cabinet mounting. Four of these brackets are required for fixed installation.

2-15. Figure 2-4 also shows an outline drawing of a type B bracket required for MT-686 rack mounting. Four of these brackets are required for fixed installation.

2-16. Similar brackets may be fabricated for installation in other equipment enclosures by modifying the type A or type B brackets as appropriate.

2-17. INPUT POWER CONNECTIONS. The receivers are shipped from the factory with their input power connections strapped for 120 vac. To utilize an input voltage of 105, 210, or 240 volts it is necessary to change the strapping arrangement on the power supply. Remove the top cover by loosening six captive 6-32 flat head, Phillips head retaining screws. Remove power supply terminal strip top cover by loosening two 4-40 pan head, Phillips head screws.

CAUTION

Observe strapping arrangement on underside of cover and verify that input power transformers are correctly strapped for the specific installation voltage. Figure 2-3 illustrates strapping arrangement. The ac line must always be connected to pins 1 and 5. This is a factory connection. DO NOT CHANGE.

Print voltage rating on space provided on receiver top covers, and replace power supply terminal strip cover and receiver top cover.

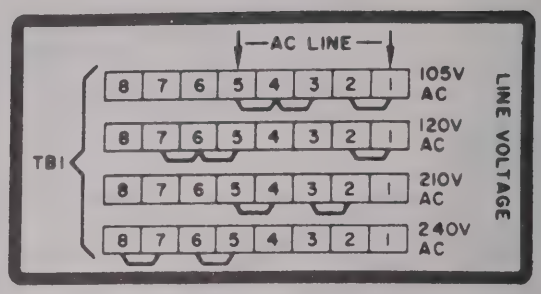


Figure 2-3. Strapping Arrangement

2-18. After the receiver slides have been firmly attached to the rack rails, connect the provided cables to their corresponding connectors at the rear of the chassis. Make sure the type N shorting connector is in place on A7J2; carefully slide the receiver into the rack observing that all cables have clearance and are not pinched or damaged. The two slots at each end of the panel allow the entry of hold-down screws into the rack. This completes installation of the receivers.

NOTE

The following paragraph is applicable only in early configuration receivers containing AGC/Squelch Module P/N 8004239G1 which requires the AUDIO MAIN ADJ control to be fully clockwise to obtain audio compression. The new configuration AGC/Squelch Module, P/N 8008586G1, will have audio compression at any setting of the AUDIO MAIN ADJ control. Therefore, it is not necessary to use an external pad or attenuation network as defined in the following paragraph.

2-19. The audio compressor stage is factory aligned to operate at +20 dbm output. Connection to audio lines requiring a different output level must be accomplished by means of external pads. The following is a diagram of a symmetrical 600 ohm "0" pad together with the formula for calculating desired attenuation in db.

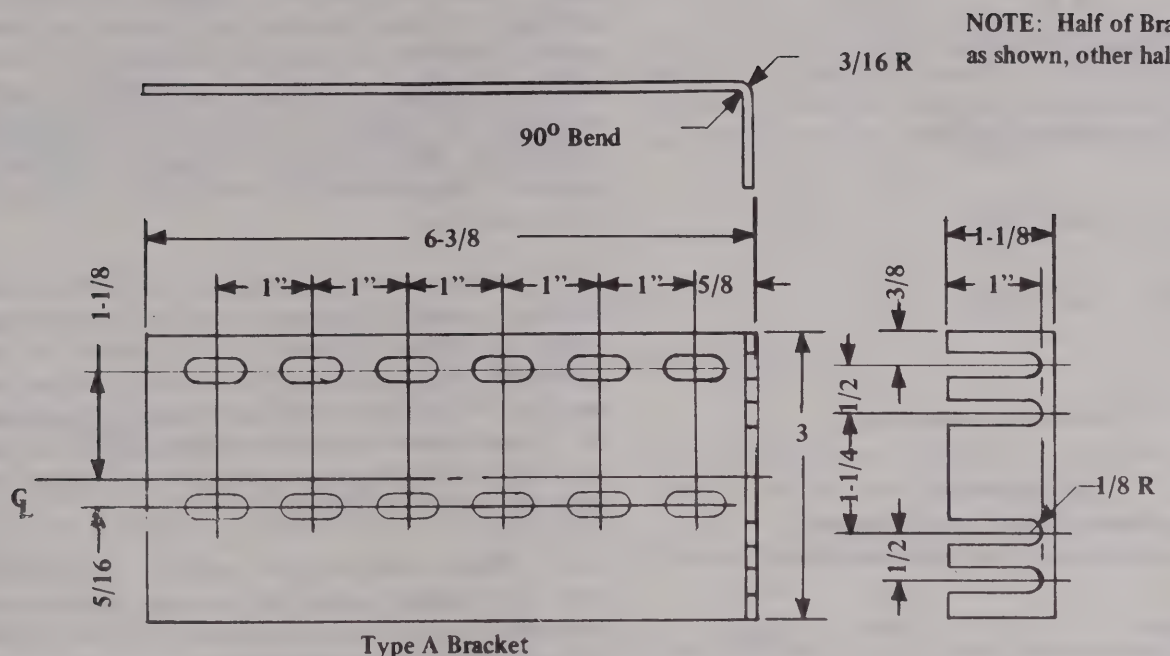
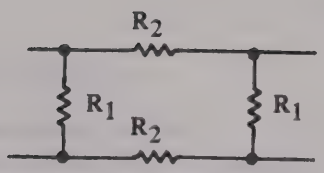


Figure 2-4. Mounting Brackets



$$R_2 = 600 \left(\frac{K^2 - 1}{4K} \right)$$

$$R_1 = 600 \left(\frac{K + 1}{K - 1} \right)$$

$$K = \log^{-1} \left(\frac{a}{20} \right)$$

a = desired attenuation in db

Typical Values
(use closest standard value available)

Attenuation (db)	K	R_1 Ohms	R_2 Ohms
0	1	∞	0
10	3.16	1155	426
15	5.6	861	813
20	10.0	733	1485
25	17.7	671	2646
30	31.6	639	4735
35	56.0	622	8397

2-20. TUNEUP AND TEST.

2-21. After completing the installation procedure of paragraph 2-12 and assuming the receiver has been properly tuned to the required operating frequency, perform the starting, operating and stopping procedure of paragraph 3-6 referring to the control and indicator functions of table 3-1. It is necessary to perform a complete tuning procedure for each change of channel or received frequency.

2-22. Both the VHF receiver and the UHF receiver have been completely aligned at the factory and should require no further alignment. If performance is not satisfactory after completing the starting procedure of paragraph 3-6 recheck the tuning procedure of paragraph 3-8. If performance is still not satisfactory refer to the fault isolation and alignment procedures of Chapter 5 to locate and correct the trouble.

2-23. When connecting two receivers for operation from one antenna perform the operating procedure in paragraph 3-15, and refer to figures 3-5 and 3-6 for proper cable length versus frequency.

SECTION IV

PREPARATION FOR RESHIPMENT

2-24. GENERAL.

2-25. The preferred method of packing for reshipment is to use the original shipping containers, if available. If the original packing material is not available, repack the receivers in separate cartons using an over-wrap and suitable cushioning to protect the units. Note: Slide drawer extensions and interface cable kit must be shipped with the radio set.

CHAPTER 3

OPERATION

3-1. INTRODUCTION. This chapter contains operation information and instructions for the VHF receiver and the UHF receiver. All operation information is identical for both receivers. The chapter is divided into three sections. Section I illustrates and describes the functions of all controls, indicators, and interlocks. Section II provides operating instructions. Starting, operating, tuning and stopping procedures are provided. Section III contains Emergency Operation procedures.

SECTION I

CONTROLS AND INDICATORS

3-2. GENERAL.

3-3. This section contains illustrations and tables to identify and describe the functions of all controls and indicators.

3-4. Controls and indicators are listed and defined in table 3-1 and illustrated in figure 3-1.

3-5. No interlocks are used in the receivers.

Table 3-1. Controls and Indicators

CONTROL OR INDICATOR	REF DES	FUNCTION
POWER		
ON-OFF		
Toggle Switch	S2	When placed in ON position provides primary input power to receiver.
Indicator Lamp	DS1	Illuminates when POWER ON-OFF switch is in the ON position.
AC FUSE (left)	F1	Two 1-ampere fuses in 105-120 vac line. Indicating fuse holders glow when fuse is blown.
AC FUSE (right)	F2	Two 0.5-ampere fuses in 210-240 vac line. Indicating fuse holders glow when fuse is blown.
F02A250V3A BAT	F3	Single 3-ampere fuse in positive side of battery input. Indicating fuse holder glows when fuse is blown.
AUDIO		
SQUELCH ADJ		
Screwdriver Adjust	R1	Sets squelch threshold level.
ON-OFF		
Toggle Switch	S1	When ON-OFF switch is in ON position squelch is operative. With switch in OFF position squelch is disabled.

Table 3-1. Controls and Indicators (Cont.)

CONTROL OR INDICATOR	REF DES	FUNCTION
MAIN ADJ		
Screwdriver Adjust	R2	Adjusts level of audio output at rear panel connector.
PHONE ADJ		
Knob Adjust	R3	Adjusts level of audio at front panel OUTPUT jack.
OUTPUT	J14	Provides audio output for headphone monitoring. (Mating plug to J14 is PJ055B).
RECEIVER INPUT	J11	Provides front panel disconnect of antenna from receiver input. Provides for signal generator input when tuning receiver.
ANTENNA	J12	
The following controls are behind the front panel access door.		
Tunable Filter Module		
IN		
Screwdriver Adjust	C1	Tunes input cavity for peak output.
OUT		
Screwdriver Adjust	C2	Tunes output cavity for peak output.
Oscillator Module		
OSC		
Screwdriver Adjust	C3	Tunes crystal oscillator for peak output.
BUF		
Screwdriver Adjust	C13	Tunes buffer for peak output.
	VHF UHF	
Mixer/Muliplier Module		
ANT		
Screwdriver Adjust	C1 C30	Tunes rf amplifier for peak output.
RF		
Screwdriver Adjust	C9 C35	Tunes mixer for peak output.

Table 3-1. Controls and Indicators (Cont.)

CONTROL OR INDICATOR	REF DES VHF	REF DES UHF	FUNCTION
LEVEL ADJ			
Screwdriver Adjust	R26	R17	Sets multiplier injection level into mixer.
*AMPL			
Screwdriver Adjust		C27	Tunes third section of multiplier for peak output.
BUFFER			
Screwdriver Adjust	C29	C11	Tunes second section of multiplier for peak output.
QUAD (UHF)		C12	
DBLR (VHF)	C24		
Screwdriver Adjust			Tunes first section of multiplier for peak output.
Rear Panel Connectors			
AC Input	J1		Provides input for ac voltage to receiver.
Signal	J2		Provides for signal input and output.
IF Output	J10		Provides for if output.
Antenna Input	J13		Provides antenna input.
Secondary Receiver Output	A7J2		Provides for secondary receiver output.
(Oscillator-Synthesizer) Thumbwheel Switches	S1,S2,S3,S4		Selects operating frequency of oscillator-synthesizer.
Oscillator-Multiplier			
FREQ ADJ	C3		Frequency fine tune
OSC	C10		Frequency tune
BUF	C16		Frequency tune
AMPL	C21		Frequency tune

* This Control Not on VHF Module.

SECTION II

OPERATING INSTRUCTIONS

3-6. STARTING, OPERATING, AND STOPPING PROCEDURE.

3-7. STARTING PROCEDURE. Verify that the input power transformer is correctly strapped for the installation voltage as indicated in paragraph 2-17, CAUTION note. Replace power supply terminal strip cover and secure with two 4-40 pan head Phillips screws. Replace receiver top cover and secure with six captive 6-32 Phillips flat head retaining screws. To turn on either of the receivers, place the POWER ON-OFF switch on the receiver front panel to the ON position, and observe the following:

1. The POWER indicator lamp illuminates.
2. After a 30-minute warmup period (5 minutes when using oscillator-synthesizer) during which the frequency controlling elements stabilize, the receiver is ready for operation, providing the tuning procedure has been completed for the operating frequency desired.

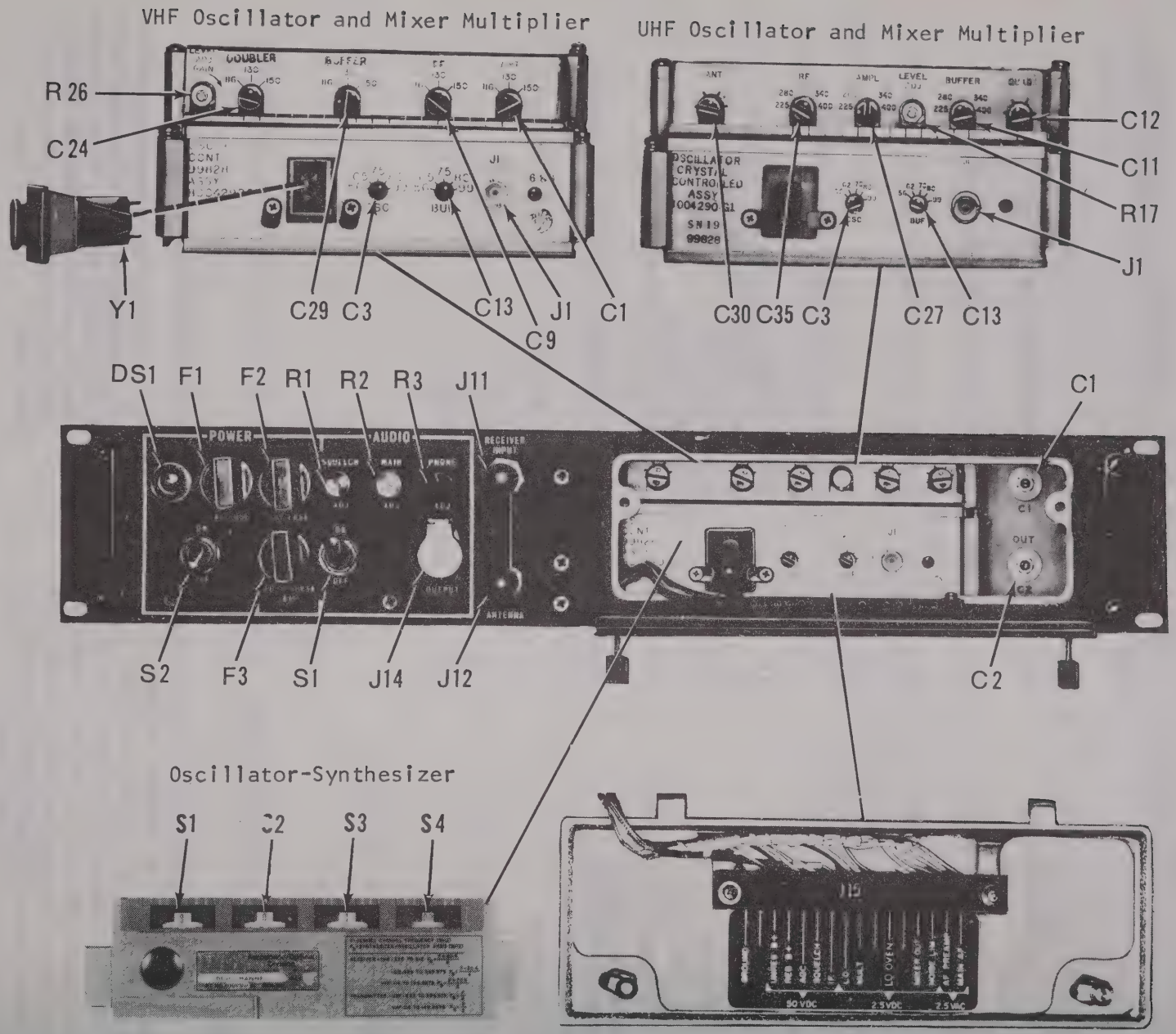


Figure 3-1. VHF Receiver and UHF Receiver Controls and Indicators

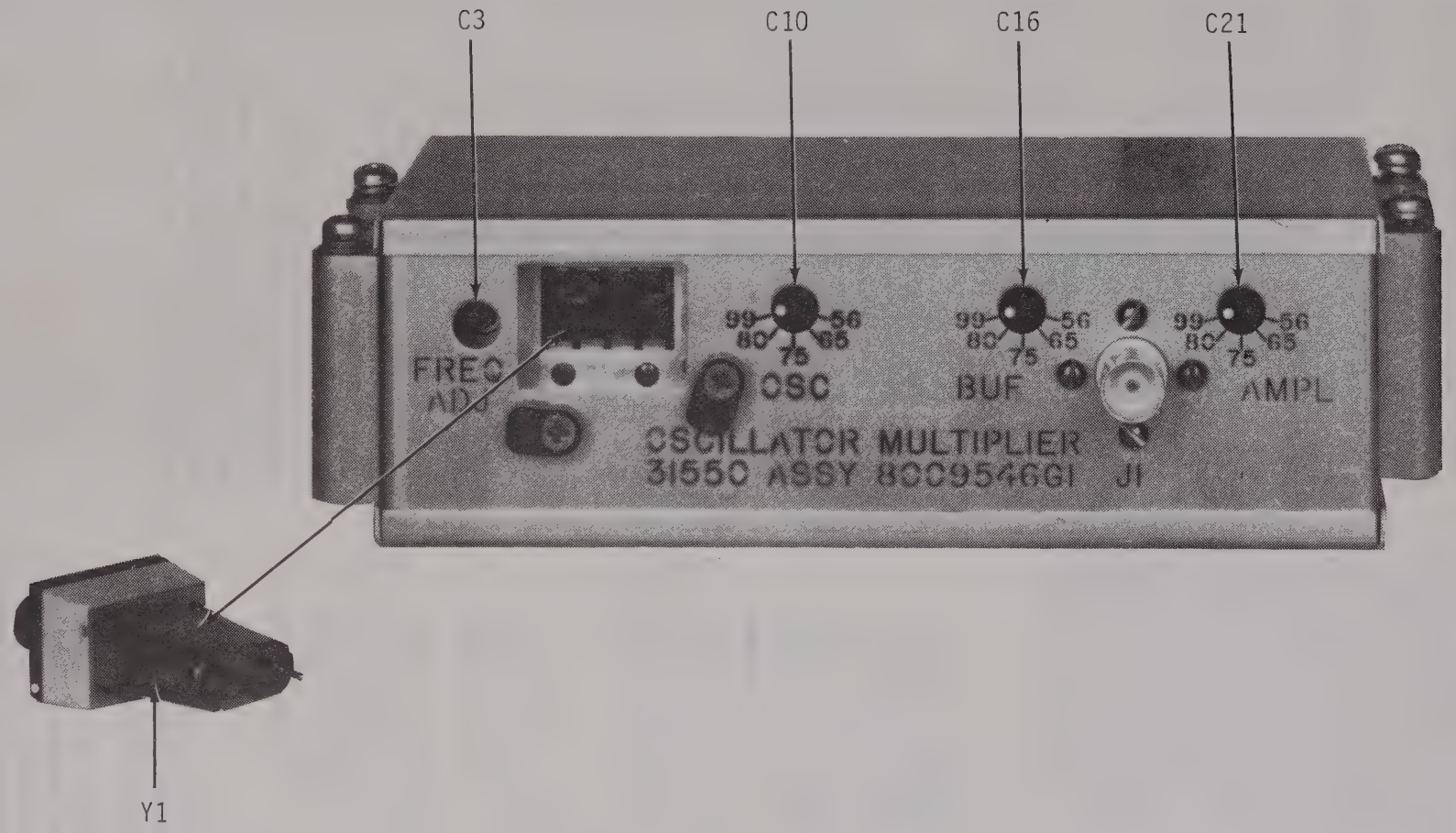


Figure 3-1A. VHF Receiver and UHF Receiver Controls and Indicators
(Oscillator-Multiplier Module Only)

3-8. TUNING PROCEDURE.

NOTE

The following tuning procedure assumes use of the crystal oscillator. If an oscillator-synthesizer is used, set the thumbwheel switches on the oscillator-synthesizer to the frequency determined by Table 3-2A and disregard the instructions on crystal oscillator adjustment.

CAUTION

Care must be exercised when inserting or removing the crystal holder. Be sure pins are properly aligned. Do not twist holder when inserting or removing as bent or misaligned pins may result.

3-9. VHF CRYSTAL SELECTION G1, G2 AND G3 OSCILLATOR. The VHF receiver is capable of operation on any of 680 channels spaced 50 khz between 116.0 mhz and 149.95 mhz. The local oscillator crystal frequency for all channels of the VHF receiver is equal to one-half the sum of the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency). Use the information contained in table 3-2 to determine the crystal frequency.

3-10. UHF CRYSTAL SELECTION G1, G2 AND G3 OSCILLATOR. The UHF receiver is capable of operation on any one of 3500 channels spaced 50 khz between 225.00 mhz and 399.95 mhz. The local oscillator crystal frequency for channels between 225.00 mhz and 312.00 mhz is equal to one-fourth the sum of the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency). The local oscillator crystal frequency for channels between 312.05 mhz and 399.95 mhz is equal to one-fourth the difference between the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency). Use the information contained in table 3-2 to determine the crystal frequency.

3-10A. VHF CRYSTAL SELECTION-OSCILLATOR-MULTIPLIER. The same procedure is used as in paragraph 3-9 except the oscillator frequency is equal to one-tenth the sum of the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency). Use the information contained in table 3-2B to determine the crystal frequency.

3-10B. UHF CRYSTAL SELECTION-OSCILLATOR-MULTIPLIER. The same procedure is used as in paragraph 3-10 except the oscillator frequency for channels between 225.00 mhz and 312.00 mhz is equal to one-twentieth the sum of the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency) and for channels between 312.05 mhz 399.95 mhz the oscillator frequency is equal to one twentieth the difference between the desired receiving frequency and 20.6 mhz (the receiver intermediate frequency). Use the information contained in table 3-2B to determine the crystal frequency.

3-11. UHF RECEIVER TUNING AND POST TUNING CHECKOUT. After selecting the proper crystal for the desired operating frequency, place it in the crystal holder as shown in Figure 3-1 and insert into the oscillator module located behind the access door on the receiver front panel.

NOTE

Before starting the UHF tuning procedure be sure that the shorting cap is on A7J2 on the rear of the receiver (Figure 2-2) and that the UHF antenna coupler, tunable filter, and mixer multiplier modules are properly installed in the receiver. See Chapter 5, Section I for module removal and replacement procedures.

Place POWER ON-OFF switch to the ON position, observe that POWER indicator lamp is illuminated and allow 30 minutes for crystal oven stabilization before proceeding with the following tuning procedure.

NOTE

If an oscillator-multiplier module is used disregard Steps a through f and refer to Paragraph 3-17E.

a. Using a screwdriver, position the dots on the oscillator module to line up with the crystal frequency markings. On the Mixer Multiplier, position the dots on the ANT and RF controls to the operating frequency. Position the QUAD, BUFFER, and MULT to the multiplier frequency (see Table 3-2).

NOTE

Careful initial setting of the mixer controls is important to avoid subsequent tuning to a wrong harmonic of the oscillator.

b. Refer to Figure 3-2 for setting the tunable filter IN and OUT controls and carefully adjust each as indicated.

c. Set HP 427A voltmeter to 1.0 Vdc scale and connect between GROUND and LO test point.

d. On the oscillator module adjust the OSC control for maximum voltmeter indication. (G1 and G2.)

e. On the oscillator module adjust the BUF control for maximum voltmeter indication. (G1 and G2.)

Table 3-2. Crystal Oscillator Frequency Determination

RECEIVER	RECEIVER FREQUENCY	CRYSTAL FREQUENCY
VHF	116.00 MHz to 149.95 MHz	$\frac{\text{Received Frequency (MHz)} + 20.6}{2}$
UHF	225.00 MHz to 312.00 MHz	$\frac{\text{Received Frequency (MHz)} + 20.6}{4}$
UHF	312.05 MHz to 399.95 MHz	$\frac{\text{Received Frequency (MHz)} - 20.6}{4}$

Table 3-2A. Oscillator-Synthesizer Frequency Determination

RECEIVER	RECEIVER FREQUENCY	CRYSTAL FREQUENCY	MULTIPLIER FREQUENCY
VHF	116.00 MHz to 143.95 MHz	$\frac{\text{Received Freq (MHz)} + 20.6}{2}$	Received Freq (MHz) + 20.6
VHF	144.00 MHz to 144.4 MHz	$\frac{\text{Received Freq (MHz)} - 20.6}{2}$	Received Freq (MHz) −20.6
VHF	144.45 MHz to 149.95 MHz	$\frac{\text{Received Freq (MHz)} + 20.6}{2}$	Received Freq (MHz) +20.6
UHF	225.00 MHz to 308.45 MHz	$\frac{\text{Received Freq (MH)} + 20.6}{4}$	Received Freq (MHz) +20.6
UHF	308.5 MHz to 309.5 MHz	$\frac{\text{Received Freq (MHz)} - 20.6}{4}$	Received Freq (MHz) −20.6
UHF	309.55 MHz to 312.00 MHz	$\frac{\text{Received Freq (MHz)} + 20.6}{4}$	Received Freq (MHz) +20.6
UHF	312.05 MHz to 349.65 MHz	$\frac{\text{Received Freq (MHz)} - 20.6}{4}$	Received Freq (MHz) −20.6
UHF	349.7 MHz to 350.7 MHz	$\frac{\text{Received Freq (MHz)} + 20.6}{4}$	Received Freq (MHz) +20.6
UHF	350.75 MHz to 399.95 MHz	$\frac{\text{Received Freq (MHz)} - 20.6}{4}$	Received Freq (MHz) −20.6

Table 3-2A. Oscillator-Synthesizer Frequency Determination (Cont)

NOTE

Since the oscillator-synthesizer produces frequencies in 6.25 khz increments, it was not possible to place all the significant digits on the frequency-select dials. Therefore the dial numbers are rounded off to the nearest channel but the module will produce only valid channel frequencies.

DIAL FREQUENCY	ACTUAL FREQUENCY
99.993 mhz	99.99375 mhz
99.987	99.98750
99.981	99.98125
99.975	99.97500
99.968	99.96875
99.962	99.96250
99.956	99.95625
99.950	99.95000
99.943	99.94375
99.937	99.93750
99.931	99.93125
99.925	99.92500
99.918	99.91875
99.912	99.91250
99.906	99.90625
99.900	99.90000

Table 3-2B. Crystal Oscillator Frequency Determination Oscillator-Multiplier

RECEIVER	RECEIVER FREQUENCY	CRYSTAL FREQUENCY
VHF	116.00 mhz to 149.95 mhz	$\frac{\text{Received Frequency (mhz)} + 20.6}{10}$
UHF	225.00 mhz to 312.00 mhz	$\frac{\text{Received Frequency (mhz)} + 20.6}{20}$
UHF	312.05 mhz to 399.95 mhz	$\frac{\text{Received Frequency (mhz)} - 20.6}{20}$

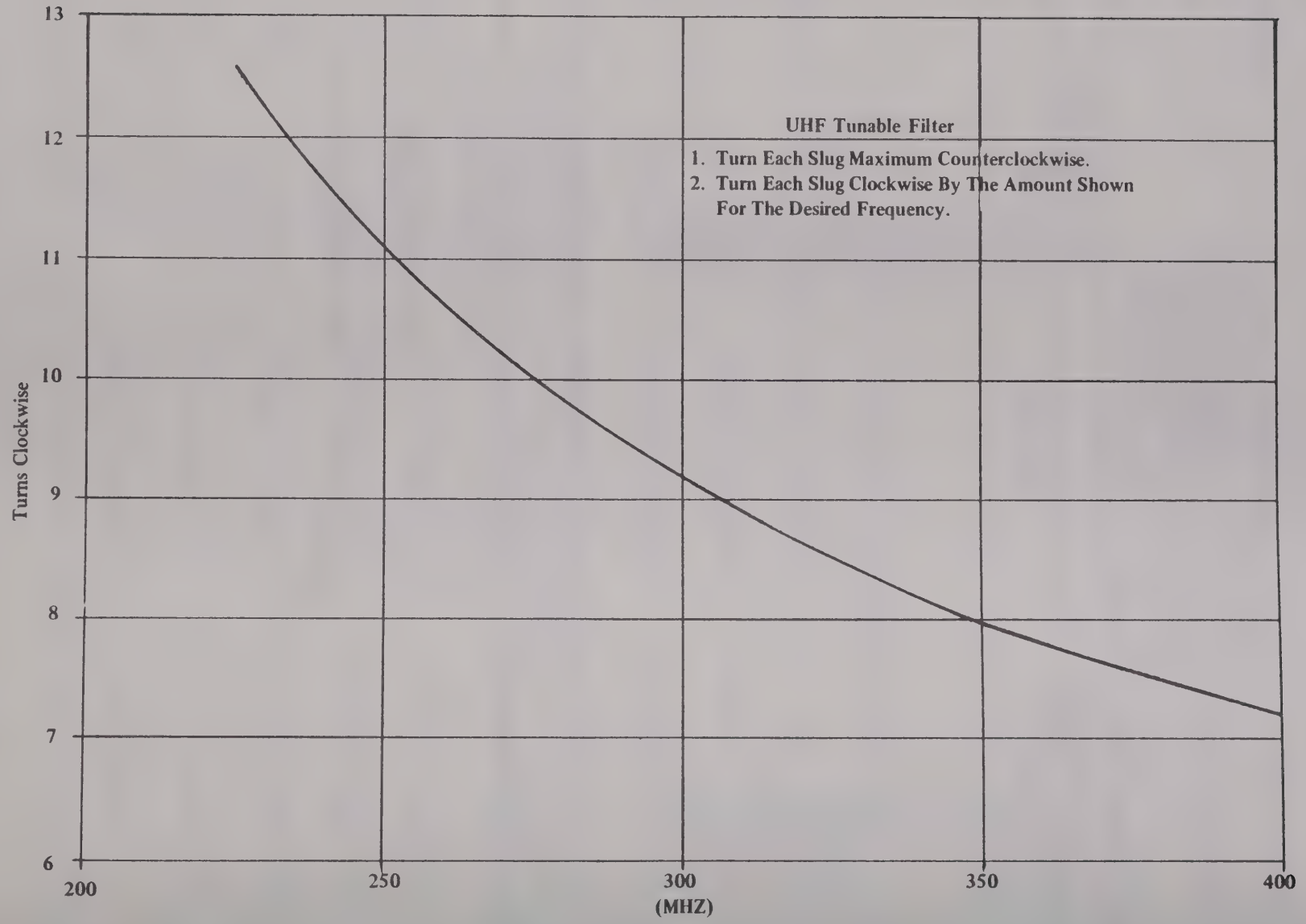


Figure 3-2. UHF Tunable Filter Turns Versus Frequency

f. Carefully readjust the OSC and BUFFER controls alternating between the two until the maximum voltmeter reading is indicated. (G1 and G2)

g. On the mixer multiplier module adjust the LEVEL ADJ control full clockwise.

h. Remove the top cover from the receiver and adjust R44 maximum counterclockwise on the noise limiter module (when used).

i. Set HP427A voltmeter to the 10 vdc scale and connect between GROUND and MULT test point.

j. Adjust QUAD, BUFFER and AMPL controls for maximum voltmeter indication. Carefully readjust the QUAD, BUFFER and AMPL controls alternately until the absolute maximum voltmeter reading is obtained. In some cases it may be necessary to change the voltmeter to the 30 volt scale.

k. Carefully adjust LEVEL ADJ control counterclockwise until the voltage indicated in table 3-3 is obtained for the desired frequency.

l. Set the voltmeter to the 10 vdc scale and connect between GROUND and AGC test point.

NOTE

Signal generator frequency should be checked at periodic intervals to assure that signal generator is on frequency.

m. Remove the connector on the front panel between ANTENNA and RECEIVER INPUT.

n. Place the SQUELCH switch to the OFF position.

o. Adjust signal generator for 30% ± 1% modulation at 1 khz ± 10%.

p. Adjust signal generator for maximum output, but not more than 1 volt (+13 dbm).

Table 3-3. UHF Receiver, Multiplier Injection Voltage Levels

FREQUENCY RANGE (MHZ)	INJECTION LEVEL (VOLTS)
225.00 to 260.00	2.5 ± 0.1
260.05 to 320.00	2.0 ± 0.1
320.05 to 340.00	2.5 ± 0.1
340.05 to 360.00	3.0 ± 0.1
360.05 to 380.00	3.5 ± 0.1
380.05 to 400.00	4.0 ± 0.1

q. Connect signal generator output to frequency counter and accurately tune the signal generator to the operating frequency of the receiver. Connect the signal generator to receiver input on front panel.

r. Adjust tunable filter IN and OUT controls for maximum voltmeter indication. Carefully readjust the IN and OUT controls alternately until the maximum voltmeter reading is obtained.

s. Reduce the signal generator output to −50 dbm (700 μv) ± 0.5 dbm.

t. Connect signal generator output to frequency counter and check for frequency accuracy. Retune if necessary. Reconnect signal generator to receiver input.

u. On the mixer multiplier module adjust the RF control for maximum voltmeter indication.

v. On the mixer multiplier module adjust the ANT control for maximum voltmeter indication.

w. Keep reducing the signal generator output and repeating steps r, t, u, and v, as required to obtain the absolute maximum voltmeter indication. Make the last round of adjustments at −97.5 dbm (3.0μ v) ± 0.5 dbm.

NOTE

If −97.5 dbm (3.0 μv) ± 0.5 dbm cannot be obtained in a maximum of three steps, refer to Chapter 5, table 5-4.

x. Set the signal generator to -97.5 dBm (3.0 μv) ± 0.5 dBm 30 ± 1% modulation at 1 KHz ± 10%. Set the voltmeter for 0.3 Vac at full scale and connect the ac probe between the IF and GROUND test points. Adjust AGC ADJUST (R7) through top cover for 125 mv ± 5 millivolts; this setting may be changed later.

y. Set the voltmeter on the 10 Vdc scale, and reconnect voltmeter to AGC test point. Reduce the signal generator level to -120 dbm (0.224 μv) ±1 dbm. The AGC voltage should drop to its quiescent value of 2.9 Vdc ±0.3 volt. If it does not drop, set signal generator power level to -120 ±1 dbm and adjust AGC ADJUST through top cover until AGC voltage just drops to its quiescent state of 2.9 Vdc ±0.3 volt. Set the signal generator level to -102 dbm (1.78 μv) ±1 dbm. The AGC voltage should be 5.0 volts or greater. Set the signal generator level for -97.5 dbm (3.0 μv) ±0.5 dbm, 30 ± 1% modulation at 1 kHz ± 10%. The 125 mv ±5 millivolt reading obtained in step x may now read between 120 and 180 millivolts.

z. Set the signal generator to -97.5 dbm (3.0 μv) ±0.5 dbm, 30% ± 1% modulation at 1 kHz ± 10%.

NOTE

If the receiver has an early configuration AGC/Squelch module, P/N 8004239G1, continue tuning procedure at step aa. If the receiver has the later configuration AGC/Squelch module, P/N 8008586G1, continue the tuning procedure at step ab.

aa. To tune early configuration AGC module, set the voltmeter to the 3 vac scale and connect between the MAIN AF test point and ground. Adjust the AUDIO MAIN ADJ level control on the front panel of the receiver maximum clockwise. The voltmeter should indicate about 1.5 to 2.0 volts. If the voltage is not within limits, adjust AF PREAMPL ADJ (R32) on top cover of the receiver. This completes the tuning of the early configuration AGC module, continue tuning precedure at step aj.

ab. To tune the later configuration AGC module remove receiver top cover and adjust Compression Level (R41) control maximum clockwise.

ac. Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND on back of front panel door. Adjust AUDIO MAIN ADJ level control on front panel of receiver maximum clockwise.

ad. Adjust AF PREAMPL ADJUST (R32) for 2.00 vac $\pm$ 25 millivolts.

ae. Adjust AUDIO MAIN ADJ level control on front panel of receiver for 1.6 vac $\pm$ 25 millivolts.

af. Adjust PREAMPL ADJUST (R32) for 2.00 vac $\pm$ 25 millivolts.

ag. Adjust Compression Level (R41) control for 1.95 vac $\pm$ 10 millivolts.

ah. Increase signal generator percent modulation from 30% to 90%. Test voltage shall remain within 1.75 to 2.45 volts. Return signal generator to 30% modulation.

ai. This completes the tuning of the later configuration AGC module, continue tuning procedure at step aj.

aj. Adjust the AUDIO MAIN ADJ level control on the front panel for 1.0 vac, set the voltmeter to the 1 vac scale. Note this reading on the db scale of the voltmeter. Switch the signal generator to the CW mode. The voltmeter should drop 10 db or more if the receiver has been properly tuned. Note the change in db. This is the signal-plus-noise ratio (S+N/N). (See 3-17B for G3 Oscillator.)

NOTE

Perform step ak only if the receiver contains a noise limiter module. If the noise limiter is not present, continue tuning either at step al. for early configuration AGC module or step am. for later configuration AGC module.

ak. Set R44 on the noise limiter module to approximately mid range. Switch the signal generator back to 30% $\pm$ 1% modulation at 1 khz $\pm$ 10%. Repeat the measurement of the S+N/N ratio as performed in the previous step. It is desired that this be 0.5 db less than what it was with R44 maximum counterclockwise. Adjusting R44 clockwise decreases the S+N/N ratio. Repeat the measurement of S+N/N and adjustment of R44 until the 0.5 db degradation of S+N/N is obtained.

al. After the above adjustments are completed, and whenever the receiver contains the early configuration AGC module, if audio compression is desired over the receiver input signal range, do the following:

1. Set the AUDIO MAIN ADJ control fully clockwise.
2. Refer to paragraph 2-19 to determine what pad to insert into the external circuit to obtain the desired signal level output.
3. This completes the tuning for early configuration AGC module when full range signal compression is desired.

am. Disconnect voltmeter and signal generator. Reconnect antenna connector between ANTENNA and RECEIVER INPUT on front panel. Replace top cover of receiver.

an. This completes the tuning procedure for operation on any one of the UHF channels.

3-12. VHF RECEIVER TUNING AND POST TUNING CHECKOUT. After selecting the proper crystal for the desired operating frequency, place it in the crystal holder as shown in figure 3-1 and insert into the oscillator module located behind the access door on the receiver front panel.

NOTE

Before starting the VHF tuning procedure be sure that the shorting cap is on A7J2 on the rear of the receiver (figure 2-2) and that the VHF antenna coupler, tunable filter, and mixer multiplier modules are properly installed in the receiver. See Chapter 5 Section I for module removal and replacement procedures.

Place POWER ON-OFF switch to the ON position, observe that POWER indicator lamp is illuminated and allow 30 minutes for crystal oven stabilization before proceeding with the following tuning procedure.

NOTE

If an oscillator-multiplier module is used, disregard steps a through f and refer to paragraph 3-17E.

a. Using a screwdriver, position the dots on the oscillator module to line up with the crystal frequency markings. Position the dots on the mixer multiplier module to line up with the operating frequency markings.

NOTE

Careful initial setting of the mixer controls is important to avoid subsequent tuning to a wrong harmonic of the oscillator.

b. Refer to figure 3-3 for setting of tunable filter IN and OUT controls and carefully adjust each as indicated.

c. Set HP427A voltmeter to 1.0 vdc scale and connect between GROUND and LO test point.

d. On the oscillator module adjust the OSC control for maximum voltmeter indication.

e. On the oscillator module adjust the BUF control for maximum voltmeter indication.

f. Carefully readjust the OSC and BUF controls alternating between the two until the maximum voltmeter reading is indicated.

g. On the mixer multiplier module adjust the LEVEL ADJ control full clockwise.

h. On the noise limiter (when used) adjust R44 maximum counterclockwise.

i. Set HP427A voltmeter to the 3 vdc scale and connect between GROUND and MULT test point.

j. Adjust DOUBLER and BUFFER controls for maximum voltmeter indication. Carefully readjust the DOUBLER and BUFFER controls alternately until the absolute maximum voltmeter reading is obtained.

k. Carefully adjust LEVEL ADJ control counterclockwise until the voltage indicated in table 3-4 is obtained for the desired frequency. It is important to use a high input impedance (1 megohm or higher) voltmeter for this step, such as an HP427A voltmeter so that the circuit is not loaded down and the level thus improperly adjusted.

l. Set the voltmeter to the 10 vdc scale and connect between GROUND and AGC test point.

NOTE

Signal generator frequency should be checked at periodic intervals to assure that signal generator is on frequency.

m. Remove the connector on the front panel between ANTENNA and RECEIVER INPUT.

n. Place the SQUELCH switch to the OFF position.

o. Adjust signal generator for 30% ± 1% modulation at 1 khz ± 10%.

p. Adjust signal generator for maximum output not greater than 1.0 volt (+13 dbm) output.

q. Connect signal generator output to frequency counter and accurately tune the signal generator to the operating frequency of the receiver. Connect the signal generator to receiver input on front panel. If AGC ADJUST (accessible through top cover on receiver) happens to be grossly misadjusted it is possible no indication will be obtained. If this is the case set AGC ADJUST maximum counterclockwise and then turn it slowly clockwise until the agc voltage just starts increasing.

r. Adjust tunable filter IN and OUT controls for maximum voltmeter indication. Carefully readjust the IN and OUT controls alternately until the maximum voltmeter reading is obtained.

s. Reduce the signal generator output to −50 dbm (700 μv) ± 0.5 dbm.

t. Connect signal generator output to frequency counter and check for frequency accuracy. Retune if necessary. Reconnect signal generator to receiver input.

u. On the mixer multiplier module adjust the RF control for maximum voltmeter indication.

v. On the mixer multiplier module adjust the ANT control for maximum voltmeter indication.

w. Keep reducing the signal generator output and repeating steps r, t, u, and v as required to obtain the absolute maximum voltmeter indication. Make the last round of adjustment at −97.5 dbm (3.0 μv) ± 0.5 dbm.

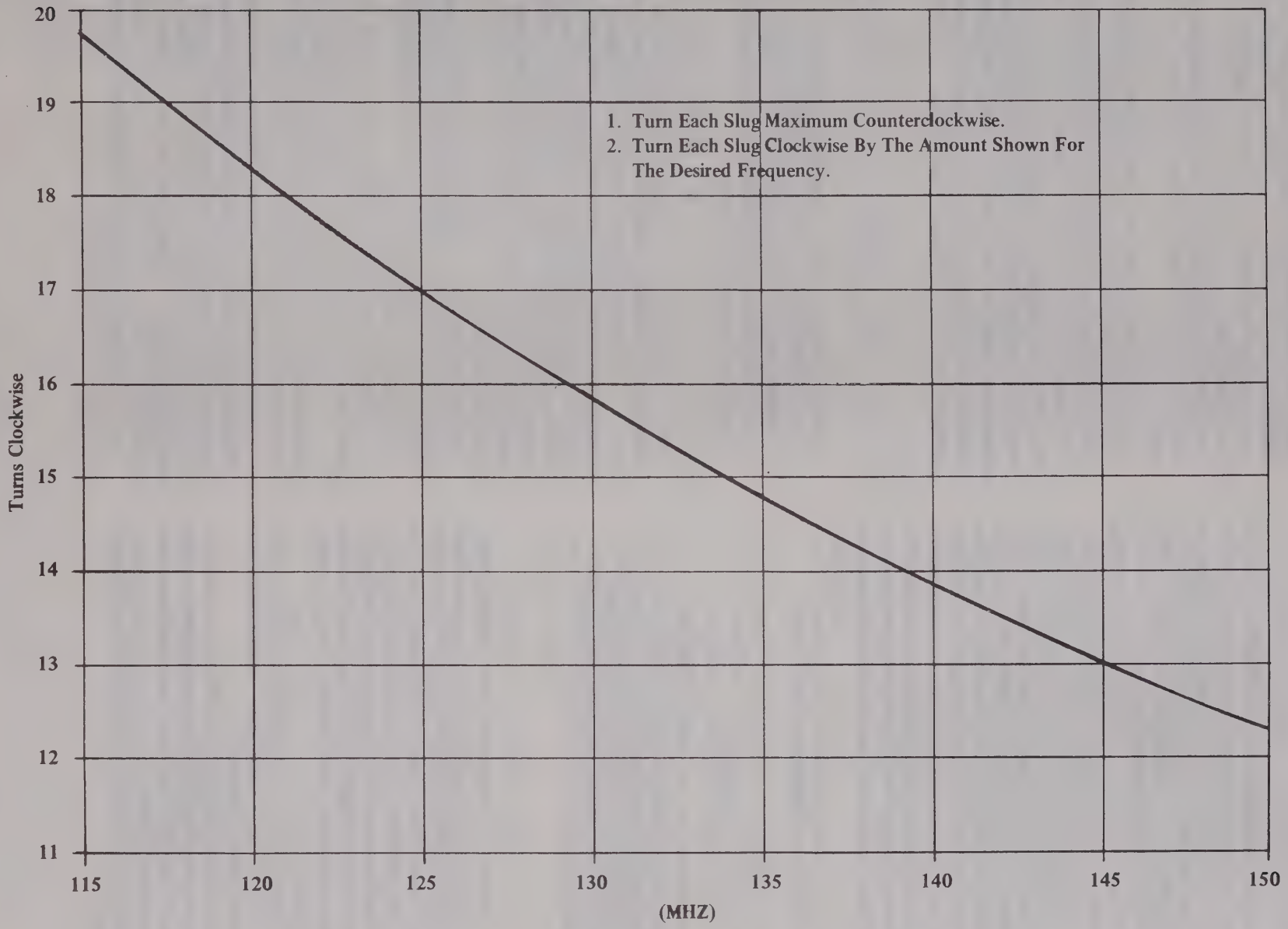


Figure 3-3. VHF Tunable Filter Turns Versus Frequency

If -97.5 dbm (3.0 μv) 0.5 dbm can be obtained in a maximum of three steps, refer to Chapter 5, table 5-4.

x. Set the signal generator to -97.5 dbm (3.0 μ v) ± 0.5 dbm 30 ± 1% modulation at KHz ± 10%. Set the voltmeter for 300 millivolts ac full scale and connect the AC probe between the IF and GROUND test points. Adjust AGC ADJUST (R7) through top cover for 125 ± 5 millivolts; this setting may be changed later.

y. Set the voltmeter on the 10 vdc scale and reconnect voltmeter to AGC test point. Reduce the signal generator level to -120 dbm (0.224 μv) ±1 dbm. The AGC voltage should drop to its quiescent value of 2.9 ± 0.3 volt. If it does not drop, set signal generator power level to -120 ± 1 dbm and adjust AGC ADJUST (R7) through top cover until AGC voltage just drops to its quiescent state of 2.9 ± 0.3 volt. Set the signal generator level to -102 dbm (1.78 μ v) ±1 dbm. The AGC voltage should be 5.0 volts or greater. Set the signal generator level for -97.5 dbm (3.0 μ v) ±1 dbm. The 125 ± 5 millivolt reading obtained in step x may now read between 120 and 180 millivolts.

z. Set the signal generator to -97.5 dbm (3.0 μ v) ± 0.5 dbm, 30% ± 1% modulation at 1 khz ± 10%

NOTE

If the receiver has an early configuration AGC/Squelch module, P/N 8004239G1, continue tuning procedure at step aa. If the receiver has the later configuration AGC/Squelch module, P/N 8008586G1, continue the tuning procedure at step ab.

aa. To tune early configuration AGC module, set the voltmeter to the 3 vac scale and connect between the MAIN AF test point and ground. Adjust the AUDIO MAIN ADJ level control on the front panel of the receiver maximum clockwise. The voltmeter should indicate about 1.5 to 2.5 volts. If the voltage is not within limits adjust AF PREAMPL ADJ on top cover of the receiver. This completes the tuning of the early configuration AGC module, continue tuning procedure at step aj.

ab. To tune the later configuration AGC module, remove receiver top cover and adjust Compression Level (R41) control maximum clockwise.

ac. Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND on back of front panel door. Adjust AUDIO MAIN ADJ level control on front panel of receiver maximum clockwise.

ad. Adjust AF PREAMPL ADJUST (R32) for 2.00 vac ± 25 millivolts.

ae. Adjust AUDIO MAIN ADJ level control on front panel of receiver for 1.6 vac ± 25 millivolts.

af. Adjust PREAMPL ADJUST (R32) for 2.00 vac ± 25 millivolts.

ag. Adjust Compression Level (R41) control for 1.95 vac ± 10 millivolts.

ah. Increase signal generator percent modulation from 30% to 90%. Test voltage shall remain within 1.75 to 2.45 volts.

ai. This completes the tuning of the later configuration AGC module, continue tuning procedure at step aj.

aj. Adjust the AUDIO MAIN ADJ level control on the front panel for 1.0 vac, set the voltmeter to the 1 vac scale. Note this reading on the DB scale of the voltmeter. Switch the signal generator to the CW mode. The voltmeter should drop 10 db or more if the receiver has been properly tuned. Note the change in db. This is the signal-plus-noise ratio (S+N/N). (See 3.17B for G3 Oscillator.)

NOTE

Perform step ak. only if the receiver contains a noise limiter module. If the noise limiter is not present, continue tuning either at step al. for early configuration AGC module or step am. for later configuration AGC module.

ak. Set R44 on the noise limiter module to approximately mid range. Switch the signal generator back to 30% ± 1% modulation at 1 khz ± 10%. Repeat the measurement of the S+N/N ratio as performed in the previous step. It is desired that this be 0.5 db less than what it was with R44 maximum counterclockwise. Adjusting R44 clockwise decreases the S+N/N ratio. Repeat the measurement of S+N/N and adjustment of R44 until the 0.5 db degradation of S+N/N is obtained.

al. After the above adjustments are completed, and whenever the receiver contains the early configuration AGC module, if audio compression is desired over the receiver input signal range, do the following:

1. Set the AUDIO MAIN ADJ control fully clockwise.

2. Refer to paragraph 2-19 to determine what pad to insert into the external circuit to obtain the desired signal level output.

3. This completes the tuning for early configuration AGC module when full range signal compression is desired.

am. Disconnect voltmeter and signal generator. Reconnect antenna connector between ANTENNA and RECEIVER INPUT on front panel. Replace top cover of receiver.

an. This completes the tuning procedure for operation on any one of the VHF channels.

Table 3-4. VHF Receiver Multiplier Injection Voltage Levels

FREQUENCY RANGE (MHz)	INJECTION LEVEL (VOLTS)
116.00 to 125.00	0.96 ± 0.1
125.05 to 134.00	1.00 ± 0.1
134.05 to 143.00	1.04 ± 0.1
143.05 to 150.00	1.07 ± 0.1

3-13. SQUELCH CONTROL ADJUSTMENT.

3-14. When it is desired to set up the squelch control on the receiver to operate at a given signal input level proceed as follows:

a. Remove the connector on the front panel between ANTENNA and RECEIVER INPUT. Connect signal generator output to RECEIVER INPUT on front panel.

b. Place the SQUELCH switch in the OFF position.

c. Set the voltmeter to the 10 Vdc scale and connect between the AGC and GROUND test points.

d. Set the signal generator power level to −97.5 dBm (3.0 μV) ± 0.5 dBm, 30% ± 1% modulation at 1 kHz ±10%.

e. Carefully adjust the signal generator fine and coarse frequency controls for maximum AGC voltage.

f. Set the voltmeter to the 30 Vdc scale and connect between the SQUELCH test point and GROUND.

g. Place the SQUELCH switch to the ON position.

h. Set the signal generator at the desired squelch level (the level must be between −97.5 dBm (3.0 μV) and −73 dBm (50.1 μV) ± 0.5 dBm), at 30% ± 1% modulation at 1 kHz ± 10%.

i. Set the AUDIO SQUELCH ADJ potentiometer maximum clockwise. The receiver will be squelched and the voltmeter should indicate less than 1 Vdc.

j. Slowly turn the AUDIO SQUELCH ADJ. potentiometer counterclockwise until the voltmeter suddenly increases approximately 8.0 volts dc (Module P/N 8008586G1) or approximately 15.0 volts dc (Module P/N 8004239G1).

k. Disconnect the signal generator and replace the connector between the ANTENNA and RECEIVER INPUT jacks on the front panel of the receiver.

3-15. OPERATING TWO RECEIVERS FROM THE SAME ANTENNA.

3-16. When it is desired to operate two receivers from a common antenna proceed as follows:

a. Tune the two receivers using the tuning procedure indicated in Paragraph 3-11 or Paragraph 3-12. The frequencies of the two receivers must be separated by 1.0 MHz or more if they are VHF receivers and 3.0 MHz or more if they are UHF receivers.

b. Connect the two receivers as shown in Figure 3-4. The proper length of cable between the two receivers must be used. The cable length is determined by the frequency of the primary receiver (See Figure 3-4). See Figure 3-5 or 3-6 for the proper cable length. Where more than one length is given either may be used. At the higher frequencies cable lengths become more critical for optimum receiver performance. Length is to be measured to the end of the center pin of the coaxial line. Total length should include any adapters used when the cable is not terminated with Type N connectors.

NOTE

Approximately 2.5 dB degradation in sensitivity will be experienced with two receivers connected for operation from a common antenna.

3-17. COLLOCATION REQUIREMENTS. The VHF receiver or the UHF receiver shall not have the signal-plus-noise-to-noise (S+N/N) ratio degraded to less than 8 dB for a 3 microvolt desired signal when operated near transmitter as follows:

a. Isolation (transmitter antenna port to receiver antenna port).

b. Transmitter-receiver minimum frequency separation.

Condition	VHF	UHF
a (see above)	30 dB	24 dB
b (see above)	± 3 MHz	± 7 MHz

3-17A. STOPPING PROCEDURE. To turn off either of the receivers, place the POWER ON–OFF switch on the receiver front panel to the OFF position. This completely deactivates the receiver.

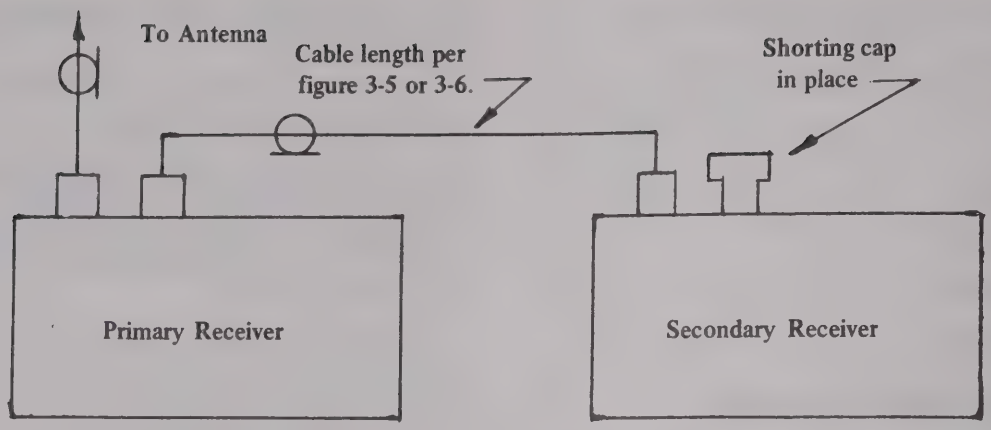


Figure 3-4. Connection For Two Receivers Operating From Common Antenna

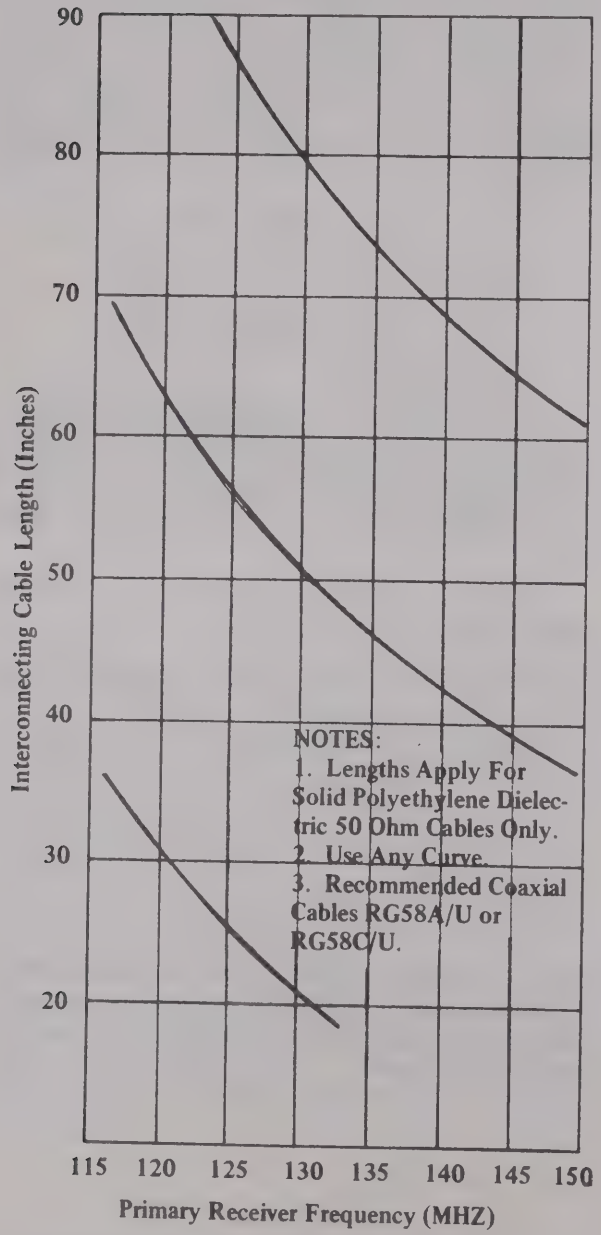


Figure 3-5. VHF Interconnecting Cable Length Vs Frequency

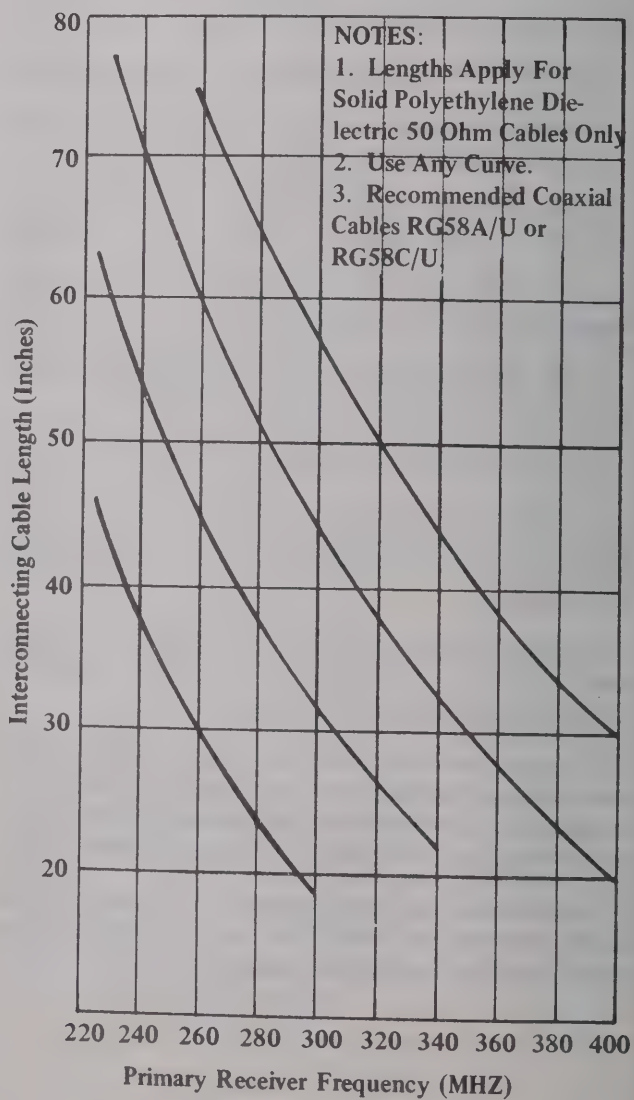


Figure 3-6. UHF Interconnecting Cable Length Vs Frequency

3-17B. G3 OSCILLATOR TUNING PROCEDURE.

3-17C. When the oscillator module A1 (G3) is used, final tuning of the oscillator is required.

3-17D. Care must be exercised when tuning at the extremes of the band (less than 65 mhz and greater than 80 mhz crystal frequency) to assure that the proper peak is used for maximum frequency accuracy. When tuning at the band edges two peaks are observable because the tuning capacitors have an adjustment range of 360° and two points exist that have the same capacitance. At the extreme low band edge, the capacitance is almost at maximum and with clockwise rotation has its capacitance decreasing. The OSC and BUF adjustments are made for maximum meter indication with the tuning capacitance decreasing. To assure proper starting position of the capacitor for frequencies less than 65 mhz and greater than 80 mhz the OSC and BUF controls are adjusted in the CW and CCW direction to observe the presence of two peaks. The peak closest to the center scale frequency marking of 75 is the correct peak. Perform initial tuning in accordance with paragraph 3.11.c through 3.11.k.

a. Carefully adjust OSC and BUF controls for a maximum reading. Care must be exercised to achieve the maximum peak observable. Note the peak reading obtained.

b. Detune the OSC control in the CCW direction then carefully adjust it in the CW direction to precisely the initial peak reading observed in step (a).

c. Detune the BUF control in the CCW direction then carefully adjust it in the CW direction to precisely the initial peak reading observed in step (a).

d. Repeat step (b). This completes tuning. If the meter reading obtainable when retuning either the OSC or BUF control is greater than or less than that reading obtained in 3.17Da, start over with 3.17Da.

(Go to note preceding paragraph 3-11.ak (UHF) or preceding paragraph 3.12.ak (VHF) and continue with the procedure.)

3-17E. OSCILLATOR-MULTIPLIER TUNING PROCEDURE.

a. Using a screwdriver, position the dots on the oscillator–multiplier module to line up with the frequency markings equivalent to 5X the crystal frequency. Position the dots on the mixer multiplier module to line up with the operating frequency markings. Refer to Figure 3-2 (UHF) or Figure 3-3 (VHF) for setting the tunable filter IN and OUT controls and carefully adjust each as indicated.

b. Set a VTVM to the 1.0 vdc scale and connect between GROUND and LO test point.

c. On the oscillator-multiplier module adjust the OSC control for maximum voltmeter indication.

d. On the oscillator-multiplier module adjust the BUF control for maximum voltmeter indication.

e. On the oscillator-multiplier module, adjust the AMPL control for maximum voltmeter indication.

f. Carefully readjust the OSC, BUF and AMPL controls alternating between the three until the maximum voltmeter reading is indicated.

NOTE

It is possible to tune the oscillator to the wrong mechanical overtone of the crystal. To verify that this has not been done, check that the final adjustment achieved for maximum output is close to the desired frequency marking.

3-17F. FREQUENCY FINE TUNE.

a. Connect a frequency counter to J1 on the front of the oscillator-multiplier unit (output signal level is approx +13 dBm).

b. With a small screwdriver or adjustment tool, adjust the FREQ ADJ control to pull the oscillator to the desired frequency.

c. Return to paragraph 3-11g for continuation of the UHF receiver tuning procedure or paragraph 3-12g for continuation of the VHF receiver tuning procedure.

SECTION III

EMERGENCY OPERATION

3-18. GENERAL.

3-19. Emergency operation of the UHF or VHF receiver is limited to two conditions.

a. Crystal not available.
b. AC power failure.

3-20. CRYSTAL NOT AVAILABLE. There are two configurations of the crystal-controlled oscillator (8004290G1, G2) and (8004290G3) that require different type connections when they are used.

NOTE

A type CR-75 crystal may be used for emergency operations, however, it may not meet the ± 0.001% frequency accuracy requirements.

3-20A. Crystal-Controlled Oscillator (8004290G1, G2) If a crystal to provide the desired operating frequency is not available, perform the following:

a. Remove crystal from holder and reinstall holder in oscillator module to maintain oven temperature.
b. Connect output of an external rf generator set to cw (HP608 or equivalent) to J1 on the oscillator module. See table 3-2 to determine setting of rf generator frequency for proper channel operating frequency.
c. Adjust external rf generator for an output to provide from 125 to 175 mv rms when terminated with a 50 ohm ± 2-ohm impedance.

NOTE

RF generator must be a stable frequency source ± 0.001% to assure optimum receiver performance. Continued monitoring for frequency accuracy is required.

d. Proceed with normal tuning procesures (paragraph 3-8).

3-20B. Crystal-Controlled Oscillator (8004290G3). If a crystal to provide the desired operating frequency is not available, perform the following.

a. Place AC POWER ON-OFF switch to the OFF position.
b. Remove receiver top cover.
c. Disconnect oscillator cable (P2) from mixer/multiplier module.
d. Remove oscillator cable (P3) from its stowage clip at rear of module and connect it to the mixer/multiplier connector (J1).
e. Secure oscillator P2 cable in stowage clip.
f. Replace receiver top cover.
g. Remove crystal from holder and reinstall holder in oscillator module to maintain oven temperature.
h. Connect output of an external rf generator set to cw (HP608 or equivalent) and to proper crystal frequency to J1 on the oscillator module. See table 3-2 to determine setting of rf generator frequency for proper channel operating frequency.
i. Adjust external rf generator for an output of from 0.5 to 1.0 volt rms when terminated with a 50-ohm ± 2-ohms impedance.

NOTE

RF generator must be a stable frequency source, ± 0.001% to assure optimum receiver performance. Continued monitoring for frequency accuracy is required.

j. Proceed with normal tuning procesures (paragraph 3-8).

3-20C. EXTERNAL FREQUENCY CONTROL (OSCILLATOR-MULTIPLIER)

3-20D. Provision is made to inject an externally generated frequency should a crystal of the desired frequency not be available.

a. Remove all power from the receiver or exciter containing the oscillator-multiplier module.
b. Remove crystal holder from oscillator-multiplier module observing caution noted in paragraph 3-8.
c. Connect the output of an rf generator at approximately +13 dbm level to J1 on the front panel of the oscillator-multiplier module. This injected frequency must be 5 times the frequency of the crystal frequency determined by previous instructions.
d. Tuning is accomplished by peaking the AMPL control, then checking the BUF and OSC controls. A dip may appear when tuning the BUF control. The dip is not wanted and this control must be tuned to peak along with the OSC control.

3-21. AC POWER FAILURE. If a 24-volt battery is already properly connected to the receiver, and an ac power failure occurs, switchover to the battery is automatic. If a battery is not connected, proceed as follows:

a. Place receiver POWER ON-OFF switch to OFF.
b. Connect 24-volt battery to rear panel connector J2, positive terminal to pin A and negative terminal to pin B or H.
c. Place receiver POWER ON-OFF switch to ON. Normal operation will be restored for a minimum period of 15 minutes from a fully charged battery.

CHAPTER 4

PRINCIPLES OF OPERATION

4-1. INTRODUCTION. This chapter provides information on the principles of operation of the VHF receiver and the UHF receiver. The chapter is divided into two sections. Section I describes the principles of operation of the receivers to a functional block diagram level. Section II discusses the principles of operation of the receivers based on the functional operation of the electronic circuits.

SECTION I

FUNCTIONAL SYSTEM OPERATION

4-2. GENERAL.

4-3. The VHF receiver and the UHF receiver are identical except for their frequency determining characteristics. These functions and those functions common to both are described to a functional system block diagram level in this section.

4-4. FUNCTIONAL DESCRIPTION.

4-5. The VHF receiver and the UHF receiver are single conversion, crystal controlled superheterodynes. (See figure 4-1.) The receivers are identical in physical configuration but different electrically in the antenna coupler, the tunable filter, and the mixer-multiplier modules.

4-6. The antenna input is fed to the antenna coupler which provides the capability of operating two receivers from a single antenna. The tunable filter provides preselection on the operating frequency. The local oscillator is crystal controlled in a temperature controlled oven. The mixer-multiplier stage doubles (VHF) or quadruples (UHF) the local oscillator frequency and heterodynes the resultant signal with the received signal to produce a 20.6 mhz intermediate frequency. The mixer-multiplier output is fed to a buffer amplifier stage which provides isolation and impedance matching for the crystal filter, or to a noise limiter stage (see paragraphs 4-10, 4-46 and 4-49).

4-7. The signal from the noise limiter or buffer amplifier is fed to a 20.6 mhz crystal filter which establishes the receiver selectivity. Four stages of intermediate frequency amplification follow the crystal filter providing a minimum of 94 db gain. After detection, the signal is fed to the audio frequency preamplifier where it is amplified and a dual output is fed to the audio amplifier for further amplification providing 100 mw of audio output to the phone jack and 100 mw of audio output to the main audio output for remote speaker operation. Automatic gain control is obtained by sampling the detected carrier level voltage, amplifying it and applying this voltage to the mixer multiplier and if amplifier. The agc voltage is also fed to the squelch stage to quiet the receiver in the absence of a received signal.

4-8. The receiver power supply converts the 47 to 420 hz ac primary power to regulated and unregulated dc voltages to operate the receiver circuits. When the ac primary input is interrupted, automatic switchover is accomplished to a dc input from an external source.

4-9. OPTIONAL CAPABILITIES.

4-10. A number of options to the basic receiver configuration are available. First, for installations where radar pulse interference is objectionable, the buffer amplifier (A5) may be replaced by a noise limiter which blanks radar type pulses. Second, the normal 20.6 mhz crystal filter (FL-1) may be exchanged for a narrow bandwidth unit intended for 25 khz channel spacing. Note that the normal and 25 khz crystal filters may be used with either the noise limiter or the buffer amplifier modules in place. Frequency stability available is 0.0005%, 0.0025%, and 0.005%. Third, an oscillator-synthesizer module is available which is directly interchangeable with and replaces the crystal oscillator module. This module provides for direct dialing of the mixer multiplier input frequency.

SECTION II

FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

4-11. GENERAL.

4-12. This section provides a discussion of the circuits comprising the VHF and UHF receivers. The discussion follows a logical operational or signal flow and is presented in the same functional sequence as in the preceding section.

4-13. ANTENNA COUPLER (VHF) A7.

4-14. The antenna coupler allows two VHF receivers to operate from the same antenna. Connector A7J2 on the rear apron of the receiver allows coupling to a second VHF receiver input. The reduced sensitivity to each receiver when the two are operated with a frequency separation of 1 mhz or greater will be a maximum of 2.5 db. When not used the second receiver output from the antenna coupler must be covered with the chained shorting cap on the receiver rear panel.

4-15. ANTENNA COUPLER (UHF) A7.

4-16. The antenna coupler allows two UHF receivers to operate from the same antenna. Connector A7J2 on the rear apron of the receiver allows coupling to a second UHF receiver input. The reduced sensitivity to each receiver when the two are operated with a frequency separation of 3 mhz or greater will be a maximum of 2.5 db. When not used. the second receiver output from the antenna coupler must be covered with the chained shorting cap on the receiver rear panel.

4-17. TUNABLE FILTER (VHF) FL2.

4-18. The VHF tunable filter consists of two tuned cavity sections. Each section is tunable over a frequency range of from 116 to 150 mhz by adjusting its variable capacitor. Internal coupling is provided between the input and output sections. Insertion loss for the filter is a maximum of 5.5 db.

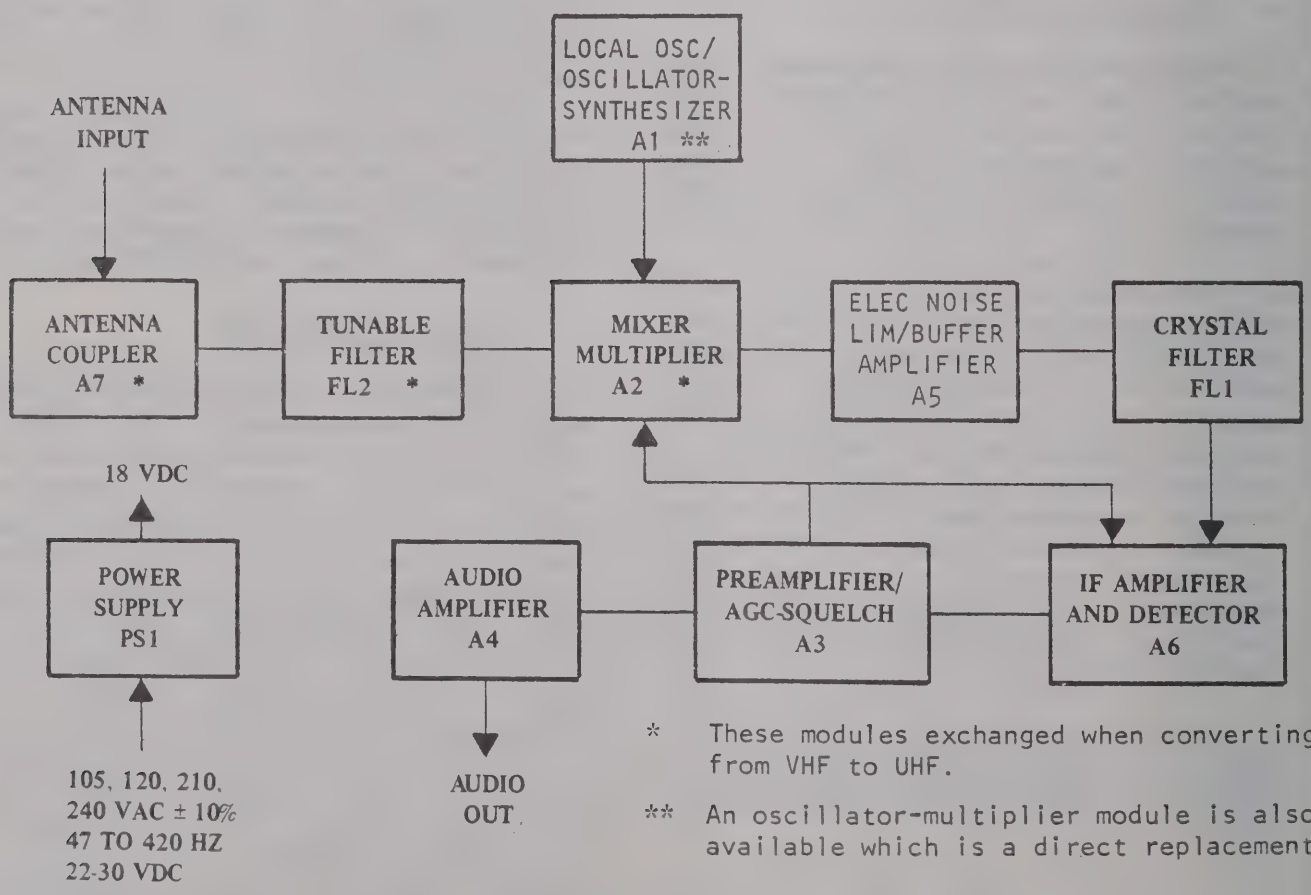


Figure 4-1. Functional Block Diagram VHF/UHF Receiver

4-19. TUNABLE FILTER (UHF) FL2.

4-20. The UHF tunable filter consists of two tuned cavity sections. Each section is tunable over a frequency range of from 225 to 400 mhz by adjusting its variable capacitor. Internal coupling is provided between the input and output sections. Insertion loss for the filter is a maximum of 5.5 db.

4-21. OSCILLATOR MODULE A1 (G1, G2).

4-22. The oscillator module consists of a crystal controlled oscillator stage, a buffer amplifier stage, and an oven with associated heaters and temperature control circuitry. See figures 6-1 and 6-2.

4-23. CRYSTAL OSCILLATOR. The oscillator stage Q1 has its base voltage held at a constant value by a voltage divider consisting of R1 and R2. Crystal Y1 is coupled to the emitter by C4 and to a tap on L2 by C6. C6 and R5 control the drive level to Y1 and also isolate it from inductive and capacitive effects of the driving circuitry. The coupling network C4 and R4 also tends to isolate the crystal. Variable capacitor C3 is tunable for resonance at the crystal frequency.

4-24. BUFFER AMPLIFIER. The oscillator stage output, from a tap on L2, is coupled through C7 to the base of buffer amplifier Q2. This stage is adjusted for resonance at the crystal frequency by variable capacitor C13. The output, from a tap on L4, is coupled through C10 and a matching pad consisting of R10 and R11 to coaxial connector P2. The signal at the junction of C10 and R10 is detected by CR1 and applied to the receiver front panel major test point LO. The signal is filtered by pi filter C11, L5, and C12 and becomes a positive voltage whose level is proportional to the oscillator output. Power supply decoupling is performed by C1, L1, C5, L3, C8, R23 and C14.

4-25. OVEN. A proportional temperature control system is utilized in the oven. The oven is maintained at a near constant temperature (75 degrees C ± 5 degrees) by heaters HR1 and HR2 and associated sensing and control circuitry. Power for the heaters is supplied by the unregulated output (22 to 39 volts dc) from the power supply module. The 22 to 39 volts is dropped through R12 and regulated at +6.2 volts at the cathode of zener diode VR1. Regulation is required at this point to allow the temperature sensing circuit to operate from a source voltage which has such a wide variation. The +6.2 volts is applied across a voltage divider made up of thermistors RT1, RT2, RT3 and potentiometer R16. R16 is used to control the oven temperature. The wiper of R16 is connected to the base of common-emitter amplifier stage Q3. The thermistors form a temperature sensing circuit. The voltage across R16 increases as the temperature in the crystal oven increases.

4-26. At power turn-on, the crystal oven will be at room temperature. The resistance of RT1, RT2, and RT3 will be high and very little voltage will be picked off R16. Q3 will then be in the cutoff region. The base drive of Q4 is controlled by R14, Q5 and R15. As the oven approaches the operating temperature, more and more voltage is applied to the base of Q3 which, driven into conduction, shunts a portion of the base drive current for Q4 to ground. This reduces the conduction of Q4 and current flow through heaters HR1 and HR2. Zener diode VR2 clamps the collector voltage of Q5 to a constant level as the 22 to 39 volt drive changes. Q5 and R19 through R22 hold the power dissipation in HR1 and HR2 constant, as the 22 to 39 vdc level changes, by controlling the base drive of Q4. The low voltage side of the heaters is brought out to the front panel major test point LO OVEN.

4-27. EXTERNAL OSCILLATOR INPUT. An external oscillator may be used in lieu of a crystal. The crystal must then be removed from the circuit and the external oscillator having an output of from 125 mv to 175 mv rms when terminated in a 50 ohm ± 2 ohm impedance connected to coaxial connector J1. The external oscillator must be adjusted to the proper frequency to serve as a local oscillator. C3 and C13 are adjusted for peak output just as they were when using a crystal.

4-27A. OSCILLATOR MODULE A1 (G3).

4-27B. The oscillator module (G3) consists of a crystal controlled oscillator stage, a buffer amplifier stage, and an oven with associated heaters and temperature control circuitry. See figure 6-2A.

4-27C. CRYSTAL OSCILLATOR. The oscillator stage Q1 has its base voltage held at a constant value by a voltage divider consisting of R1 and R2. Crystal Y1 is coupled to the emitter by C4 and to a tap on L2 by phase network Z1. Z1 controls the phase and magnitude of the drive level to Y1. Z1 and R5 isolate Y1 from inductive and capactive effects of the driving circuitry. The coupling network C4 and R4 also tends to isolate the crystal from the transistor. Variable capacitor C3 is tunable for resonance at the crystal frequency. Power supply decoupling is provided by C1, L1, C20, C14 and R23.

4-27D. BUFFER AMPLIFIER. The oscillator stage output, from a tap on L2 is coupled through C7 to the base of buffer amplifier Q2. This stage is adjusted for resonance at the crystal frequency by variable capacitor C13. The output from a tap on L4 is coupled through C10 and a matching pad consisting of R10 and R11 to coaxial connector P2. The signal at the junction of C10 and R10 is detected by CR1 and applied to the receiver front panel test point LO. The signal is filtered by pi filter C11, L5, and C12 and becomes a positive

voltage whose level is proportional to the oscillator output. Power supply decoupling is performed by C8, L3 and C5.

4-27E. OVEN. A portional temperature control system is utilized in the oven. The oven is maintained at a near constant temperature (75 degrees C ± 5 degrees) by heaters HR1 and HR2, and associated sensing and control circuitry. Power for the heaters is supplied by the unregulated output (22 to 39 volts dc) from the power supply module. R28 is the load resistor for the metering circuit and R25 is the multiplier resistor that furnishes the proper level for the LO OVEN front panel major test point. L6 and C19 furnish decoupling to the oven metering line. The regulated voltage is furnished to the resistance bridge of R13, R16, R14, R19 and RT1. Resistor R12 and R15 establish the dc operating voltage of the operational amplifier AR1. Potentiometer R16 is used to control the oven temperature and is adjusted for a temperature of 75 degrees C ± 5 degrees. With this adjustment the bridge is balanced and pin 2 and 3 of AR1 are at the same voltage. At power turn on, the oven is at room temperature. The resistance of RT1 will be high which will cause pin 3 of AR1 to be low and output of AR1 low. Transistor Q3 will be turned on by base drive through R29, R20 and VR1. With this conduction the collector current of Q3 furnishes base drive to Q4. Q4 is turned on and furnishes collector current through the heater elements HR1, HR2 from the unregulated voltage through R28. The voltage across R28 is furnished to the front panel for LO OVEN metering test point. R30 is to minimize thermal runaway resulting from Q4 operating at high temperature. As the oven approaches the operating temperature, the resistance of RT1 decreases to raise the voltage at Pin 3 of AR1 which raises the output voltage of AR1 to decrease drive to Q3 and Q4 which reduces heater current. At the operating temperature the output of AR1 is high so that Q3 is almost turned off which reduces base drive to Q4 and reduces the heater current to almost zero. VR1 assures that Q3 is turned off when heater current is not required as in the case when ambient temperatures exceed the oven temperature.

4-27F. EXTERNAL OSCILLATOR INPUT. An external oscillator may be used in lieu of a crystal. Remove receiver cover. Disconnect cable P2 of the oscillator module from the mixer/multiplier module. Remove oscillator cable P3 from its stowage clip at rear of oscillator module and connect it to the mixer/multiplier module connector J1. Secure cable P2 in stowage clip. The crystal must then be removed from the circuit and the external oscillator output connected to coaxial connector J1. The external oscillator must be adjusted to the proper frequency to serve as a local oscillator with a power level input between +7 to +13 dbm.

4-27G. OSCILLATOR-SYNTHESIZER A1

4-27H. GENERAL. The oscillator-synthesizer generates selectable stable frequencies by a voltage-tuned oscillator. The selected oscillator output frequency is fed to a prescaler counter which divides the frequency by 4 and feeds it to a variable counter. The variable counter further divides the frequency by a ratio of 9000 to 15,999 as determined by the settings of the frequency select thumbwheels. The division ratio of the counter is such that when the voltage-tuned oscillator is generating the correct frequency, the output of the variable counter is 1.5625 khz. This output signal is fed to a phase detector and compared with a 1.5625 khz reference signal. The 1.5625 khz reference signal is derived from a precision crystal-controlled oscillator and a digital fixed-frequency divider counter. The phase difference between these two signals determines the d-c voltage which controls the voltage-tuned oscillator such that phase lock with the reference oscillator is maintained. The nominal output level of the oscillator is +14 dbm ± 3 dbm. Figure 6-2B is a block diagram of the synthesizer.

4-27I. REFERENCE GENERATOR. The reference generator contains a temperature compensated crystal oscillator which provides a 3.2 mhz signal. Temperature stability is obtained without the use of an oven. A screwdriver trimmer adjustment is provided in the side of the crystal housing, covered by a removable, reusable sealed access cover. This cover is behind the hole plug located on the front of the synthesizer below the thumbwheel switches. The oscillator operates from the +20 vdc regulated. It is followed by an integrated circuit divider with straight-binary division by 2048, which operates from the +5 vdc regulated. The output from the reference generator is a square wave approximately 5 volts peak-to-peak, which is coupled to the phase comparator input. This is a solder sealed module and should not be serviced except by the manufacturer.

4-27J. DIVIDER/CONTROL. This board determines the output frequency. The board contains a prescaler (divide by 4) and a variable counter with its associated frequency selection switches. The rf sample from the rf generator board is fed through attenuator R15 and R16. C5 is a d-c block which couples the rf to the base of amplifier Q4. This device places the rf at a dc level of about 3.2 volts by virtue of bias resistors R17 and R18 which is the optimum input level for U8. U8 is an emitter-coupled logic dual-D flip-flop which is hooked up to divide the input rf signal (56.25 mhz to 99.99375 mhz) by 4. The output of U8 is fed to an emitter coupled pair Q1 and Q2. This circuit amplifies the output of U8 and shifts the signal level to that of TTL (transistor-transistor logic). Q3 is used as a saturating switch which drives the first logic gate.

4-27K. The variable counter number (divide by N), is essentially a chain of programmable counters constructed entirely with monolithic integrated circuits. The division ratio N ranges from 9000 to 15,999 and is programmed by generating binary logic levels with the 4-digit frequency selector thumbwheel switches. The first 3 switches are inverted "nines" complement binary coded decimal (bcd). Switch S4 is hexadecimal code which programs U5 (divide by 16). S1, S2, and S3 program U2, U3, and U4 respectively, which are divide by 10 counters. Assuming the thumbwheels are set to 99.993 this means all switches are made placing a "low" on all the inputs, so the division ratio is 15,999. Thus the signal is coupled through the NAND gate (U7) following Q3 and into U5. This divides the input

24.9984375 M BITS/SEC pulse train by 16. The output of U5 drives the input of U4 which divides by 10. This signal then drives U3, which drives U2, each of which divide by 10. When the counter reaches 99.99375 (by dial), and 15,997 pulses have been counted, the inputs to the U1 AND gates (6-16) are all high, which enables a 3 input AND gate of U6 (pin 3, 4 and 5). On the 15,998th pulse U6 changes state, which resets U2, U3, U4 and U5, but does not cause a pulse out of U7-6 because U7-5 only responds to a positive going input transition. On the 15,999th pulse the transition is of the proper polarity to generate a narrow pulse (approximately 10 microseconds) which drive the phase comparator. These NAND gates are used to shape the output of U6 to a narrow pulse (approximately 10 microseconds) which drives the phase comparator.

4-27L. If the thumbwheels are set to numbers other than 99.993 the inputs to the divider counters are made high through the switch. Z1 is a resistor network consisting of 15 each 4.7K ohm pull-up resistors with one lead common to pin 16 (B+). No change will occur until the data strobe drops to a logic zero (Q of U6 upon full count). At that time the data on the inputs will be transferred to their associated counters and the count will take up from there on the next clock pulse. Under these conditions, the count required will be shortened by the amount of the preset inputs.

4-27M. RF GENERATOR. The rf generator provides the output signal of the synthesizer, as well as driving the divider control prescaler. The printed wiring board contains the oscillator, limit controls for the oscillator, a buffer amplifier, a final amplifier, and a voltage regulator. The oscillator is basically a voltage-tuned Hartley circuit, with L2, CR1 and CR2 the tank. CR1 and CR2 are voltage variable capacitors (varactor diodes) whose capacity is dependent on the amount of reverse voltage. This control voltage is obtained from the output of the phase comparator, and is coupled through R29 and R3, with C22 used as a bypass. Q1 is a high-frequency field-effect transistor, with R1, R2, R35, R36 and R37 providing bias and feedback. C2, C3, C7, C26 and C27 are all bypass capacitors, and C5 and C25 are blocking capacitors. L1 is an autotransformer and is used to couple the signal out to the buffer amplifier Q2, through R4, C4 and C28.

4-27N. R10 is a d-c feedback resistor, and R9 is the collector load. L3, C11, L4 and C12 are low-pass filter sections to reduce the second harmonic, with C8, C9 and C23 used as bypasses. L5 is an autotransformer and couples the signal into a signal splitter L6. R11, R12, and R13 are used to attenuate the signal which goes back to the divider control. L7, C16 and R15 match the input impedance of Q3, the final amplifier. R18 is the d-c feedback with R17 the collector load. L8, C17, L9 and C18 are two low-pass filter sections to reduce harmonics, with C10, C15 and C24 bypasses. L10 is an autotransformer which couples the signal to C19, a d-c block. R19, R20 and R21 are used to attenuate the signal to provide isolation from loading effects of the synthesizer output. R22, CR3, C20, R23, C21, and R24 form an r-f detector which indicates the presence of rf on the receiver front panel L0 test point.

4-27O. U1 is a transistor array of two individual transistors and two transistors internally connected as a Darlington circuit. U1 is used as a voltage regulator, with VR1 the zener reference. Q4 and Q5 are used to limit the control line voltage to the oscillator. They are turned on by S1 on the divider control. This switch has binary coded decimal outputs and depends on the frequency selected by the first thumbwheel switch. Either or both Q4 and Q5 may be turned on. When either is turned on, a voltage limit is developed across the precision resistors which are coupled to the control line. This voltage over-rides the control voltage from the phase comparator and limits the oscillator range. This prevents the synthesizer from locking falsely on a harmonic.

4-27P. PHASE COMPARATOR. The phase comparator converts the difference between the phase of the variable counter and the reference generator to an error voltage. Note that the frequency of these two signals is the same, but they differ in phase. Q3 is a voltage regulator of the capacitor multiplier type. C9 and R13 are filters for the regulated 18 to 20 vdc input supply. VR1 is the zener diode which provides the reference voltage. C7 and C8 are bypass capacitors for VR1, with R11 and R12 the bias for Q3. C5, C6, and R9 are filters for the regulated output of Q3. R28 is a decoupling component to further filter the input voltage to the reference generator. R27 is the current limit for VR2, which is the zener diode voltage reference for the 5 volt supply to the reference generator. Q1 is a switch for the square wave from the reference generator. R1, R2 and C1 differentiate the leading edge of the incoming square wave to cause a quick turn on of Q1. This drives the ramp generator Q2. When Q1 conducts, it discharges C2 and C3, and pulls the base and emitter of Q2 toward ground. After Q1 turns off, C2, C3, R4, and R5 are used as an RC time constant to create a ramp. Since Q2 is an emitter follower, the output is bootstrapped back to the base to increase the ramp. R7 is used to linearize the ramp. R6 and R8 are bias resistors for Q2.

4-27Q. Q5 is a switch for the negative pulse from the divider control circuit which is differentiated by C10 and R15. R14 and R16 are bias resistors. C11 and R17 couple the leading edge of the signal to the gate of Q6 while also providing a high impedance. The ramp generator output is applied to the source of Q6 and is a varying dc voltage. When the sample pulse from the divider control is applied, Q6 conducts the d-c level that is on the source at that particular instant and this d-c level is stored on C12. This level is held until the next sample pulse. Thus the circuit "samples" the d-c level of the ramp, and "holds" it. This

"hold" voltage is a continuous voltage that is proportional to the phase difference of the two input signals. During search mode (before phase lock occurs), CR1 or CR2 conduct because there is greater than 0.6 volt across them. After phase lock occurs, the voltage differential is low and R25 provides isolation for any noise that might be present. U1 is a high input impedance operational amplifier which is used as a d-c level shifter to provide the proper d-c level for the voltage-tuned oscillator. It has almost unity gain, with R19 and R26 providing the nominal operating level. R21, C14, R22, C15, R23, C16, R24 and C18 form a multi-section low-pass filter which is used to remove any undesired a-c signal from the control voltage to the voltage-tuned oscillator. During search mode, most of the filter is bypassed by L1 and CR2 or CR3, which conduct when the voltage differential is greater than 0.6 volt.

4-27R. SWITCHING REGULATOR. This printed wiring board consists of an input filter, a power switch driver, and an output filter. The input filter, is C1, C2 and L3. U1 is the switch driver, with R3 used as a short circuit protector. R4, R5, and R6 is a voltage divider string. L1 is an inductor which filters the dc pulses from the power switch. Operation consists of U1 being turned on by the feedback sensor after it drops to a sufficiently low value. It is an operational amplifier with its own internal reference diode. It operates as a switch and is either on or off. It drives an integrated circuit mounted on the back of the synthesizer which is a power switch. This switch conducts the unregulated dc for short pulses, operating at 40 khz switching frequency. C4, C5, and L2 form an additional filter to smooth the 5 volts.

4-27S. OSCILLATOR-MULTIPLIER A1 (G1).

4-27T. GENERAL. The oscillator multiplier module consists of a crystal controlled oscillator and multiplier stage, a buffer amplifier stage and an output amplifier stage that provides the necessary drive signal to the mixer multiplier. The oscillator-multiplier requires a fundamental mode crystal operating in the frequency range of 11.25 mhz to 99.987500 mhz. (See Tuning Procedure paragraphs 3-10A and 3-10B for crystal frequency selection). The output frequency from the module is five times (X5) the crystal frequency. Figure 6-2C is a schematic of the oscillator-multiplier module.

4-27U. OSCILLATOR-MULTIPLIER. The oscillator stage Q_1 is a modified Colpitts type crystal oscillator circuit, with base bias voltage held constant by the voltage divider consisting of R_3 and R_4. Crystal Y 1 operates in an antiresonant mode, with the parallel capacitors C25, C2 and C3 controlling the operating frequency. C3 is the frequency adjust capacitor on the front panel of the oscillator multiplier, C25 is an internal adjustment set at the factory so that the output frequency is proper with C3 adjusted to mid range. This allows for plus or minus front panel adjustment of frequency for crystal having an initial error up to $\pm$ 25 parts per million (ppm). Capacitor C4 and C5 provide the oscillator feedback divider, with R_1 the transistor emitter resistor. The collector circuit of Q1 is tuned to the fifth harmonic of the oscillator, with the resonant circuit consisting of L_2 in parallel with C10 and C11, with C10 the front panel tuned element. The dc input for Q1 consists of a 12 volt regulator circuit with zener diode VR1 providing the regulator action, and R6, R1, C6 and C7 providing the necessary filtering and decoupling to isolate the oscillator stage. Resistor R2 serves as the collector current limiting resistor, and C8 serves as the RF decoupling capacitor for the tuned collector circuit. Resistor R7 and capacitor C9 provide loose coupling to the Hi Q tuned filter consisting of L4 in parallel with C15 and front panel tuned C16. This Hi Q filter circuit aids in eliminating the unwanted harmonics, and allows the fifth oscillator harmonic to pass when properly tuned.

4-27V. BUFFER AMPLIFIER. Transistor Q2 serves as a buffer emitter follower stage, with its high input resistance providing a minimum loading to the tuned circuit of L4, C15 and C16. Resistor R8 and capacitor C17 couple the filtered fifth harmonic to the base of emitter-follower Q2, R9 and R10 are bias resistors for Q2, and R11 serves as the output emitter resistor.

4-27W. OUTPUT AMPLIFIER. Transistor stage Q3 serves as the rf output stage from the oscillator multiplier. The signal is coupled to the base of Q3 through parasitic suppressor resistor R14. Emitter resistors R15 and R16 provide emitter biasing, with R15 serving as an emitter degenerating resistor to protect aginst gain variations of this amplifier due to transistor gain variations. C22 serves as emitter bypass capacitor. The collector of the rf tuned circuit consists of L3, C20 and front panel tuned C21. This stage is likewise tuned to the 5th harmonic of the oscillator. The rf output is coupled through C19 to a 2db pad consisting of R18 and R19. The pad serves as a buffer between the output stage and the circuit to be driven, and additionally serves as a resistive drive source of approximately 50 ohms to the output coaxial cable and connector.

4-27X. METERING CIRCUIT. A tuning detector circuit consisting of R17, rectifier diode CR1, rf filter C24, L6, C23 and meter scaling resistors R12 and R13 provide a dc tuning indication to the transmitter or receiver oscillator test point.

4-27Y. The dc input for Q2 and Q3 is filtered and decoupled to provide B+ isolation by components C13, C12, L1, C14 and L3. Capacitor C18 serves as the rf decoupling capacitor for the Q3 tuned collector circuit. J1, a BNC connector on the oscillator front panel, provides a frequency monitoring test point, for tuning frequency adjust capacitor C3 to the desired frequency accuracy.

4-27Z. EXTERNAL INPUT. Additionally, J1 can be used as an external signal generator input if desired. Crystal Y1 should be removed however, and it is still necessary to adjust C16 and C21 front panel tuning adjustments and observe the oscillator test point to obtain maximum output. External drive level should be 1 to 2 volts rf rms input.

4-28. MIXER/MULTIPLIER (VHF) A2 (G1).

4-29. The VHF mixer/multiplier module consists of a temperature compensated and agc controlled rf stage, a mixer stage, a local oscillator frequency doubler stage, and a buffer amplifier with a temperature compensated feedback stage. Optimum gain for the module is 12 to 14 db. See figure 6-3. The rf input from the antenna is coupled through C36 and C37 to a tap on L1. Resonance at the received frequency is achieved by adjusting variable capacitor C1. The signal from a tap on L1 is coupled through C2 to gate 1 of dual-gate field effect transistor Q1. The source of Q1 is supplied through R7 and R8 from the cathode of zener diode VR1. The +3.3 volts established by the diode, is used to raise the source of Q1 sufficiently above ground so that the gates may be negatively biased relative to the source.

4-30. This voltage at gate 2 of Q1 is developed from the agc input to the module. The agc input is divided by R1 and R2 and applied to the base of common emitter amplifier stage Q3. The agc input is also connected through L15 and PIN diode CR4 to the voltage divider R29 and R30. As the agc voltage level increases with increasing rf signal level, the PIN diode is driven into conduction and thus attenuates incoming signals and prevents Q1 and Q2 from being overdriven. The collector of Q3 becomes less positive as the input agc level becomes more positive. This voltage is a bias voltage direct coupled to gate 2 of Q1 after being level changed by zener diode VR2 allowing the agc input to control the level of the rf signal through Q1. The output at the drain of Q1 is coupled through C7 to parallel tuned circuit L3 and C9. C9 is adjustable to peak up the signal at the received rf frequency. The signal is then coupled through C10 to gate 1 of the dual-gate field effect transistor mixer stage Q2. The doubled crystal oscillator frequency is applied to gate 2 of Q2 and the intermediate frequency of 20.6 mhz is produced at the drain of Q2. Variable capacitor C41 is adjusted for maximum output at the IF signal. Impedance matching for the output circuit is provided by matching network L5, C18, C41 and C42. Temperature compensation is provided by thermistor RT3 and R36. The if signal is also detected by CR1 and applied through R15 to the receiver front panel major test point MIXER OUT as a positive voltage level.

4-31. The output from the oscillator module is coupled through C21 to the base of doubler stage Q4. This signal is 0.6 to 1.0 volt rms. Approximately a + 0.6 volt bias voltage is applied through R31 to the base of Q4. C24 is adjusted to peak up the signal in the collector of Q4 at twice the signal frequency impressed upon the base. This doubled frequency is induced from L9 into L10 and coupled through C25 to the emitter of buffer amplifier stage Q5. A feedback loop from Q6 establishes the voltage level on the base of Q5 thereby controlling the emitter-base bias of Q5 stabilizing its output. C29 is adjustable to resonate at the frequency produced by the preceding doubler stage. This output is coupled through C33 and C11 to gate 2 of mixer stage Q2 as previously discussed. The output is also detected by CR3 and applied through a low pass pi filter and R27 to the base of Q6. R26 provides level control by controlling the feedback voltage to Q5; temperature compensation is provided by RT2. The detected and filtered output is also applied through R28 to the receiver front panel MULT test point.

4-32. MIXER/MULTIPLIER (VHF) A2 (G2).

4-33. The VHF mixer/multiplier module consists of a temperature compensated and agc controlled rf stage, a mixer stage, a local oscillator frequency doubler stage, and a buffer amplifier with a temperature compensated feedback stage. Optimum gain for the module is 12 to 14 db. See figure 6-4. The rf input from the antenna is coupled through C36 and C37 to a tap on L1. Resonance at the received frequency is achieved by adjusting variable capacitor C1. The signal from a tap on L1 is coupled through C2 to gate 1 of dual-gate field effect transistor Q1. The source of Q1 is supplied through R7 from the cathode of zener diode VR1. The +3.3 volts established by the diode, is used to raise the source of Q1 sufficiently above ground so that the gates may be negatively biased relative to the source.

4-34. The voltage at gate 2 of Q1 is developed from the agc input to the module. The agc input is divided by R1 and R2 and applied to the base of common emitter amplifier stage Q3. The agc input is also connected through L15 and PIN diode CR4 to the voltage divider R29 and R30. As the agc voltage level increases with increasing rf signal level, the PIN diode is driven into conduction and thus attenuates incoming signals and prevents Q1 and Q2 from being overdriven. The collector of Q3 becomes less positive as the input agc level becomes more positive. This voltage is a bias voltage direct coupled to gate 2 of Q1 after being level changed by zener diode VR2 allowing the agc input to control the level of the rf signal through Q1. The output at the drain of Q1 is coupled through R38 and C7 to parallel tuned circuit L3 and C9. R38 is a parasitic suppression resistor. C9 is adjustable to peak up the signal at the received rf frequency. The signal is then coupled through C10 to gate 1 of the dual-gate field effect transistor mixer stage Q2. The doubled crystal oscillator frequency is applied to gate 2 of Q2 and the intermediate frequency of 20.6 mhz is produced at the drain of Q2. Variable capacitor C41 is adjusted for maximum output at the if signal. Impedance matching for the output circuit is provided by matching network L5, C18, C41, and C42. Temperature

compensation is provided by thermistor RT3 and R36. The if signal is also detected by CR1 and applied through R15 to the receiver front panel major test point MIXER OUT as a positive voltage level.

4-35. The output from the oscillator module is coupled through C21 to the base of doubler stage Q4. This signal is 0.6 to 1.0 volt rms. Approximately a +0.6 volt bias voltage is applied through R31 to the base of Q4. C24 is adjusted to peak up the signal in the collector of Q4 at twice the signal frequency impressed upon the base. This doubled frequency is induced from L9 into L10 and coupled through C25 to the emitter of buffer amplifier stage Q5. A feedback loop from Q6 establishes the voltage level on the base of Q5 thereby controlling the emitter-base bias of Q5 stabilizing its output. C29 is adjustable to resonate at the frequency produced by the preceding doubler stage. This output is coupled through C33 and C11 to gate 2 of mixer stage Q2 as previously discussed. The output is also detected by CR3 and applied through a low pass pi filter and R27 to the base of Q6. R26 provides level control by controlling the feedback voltage to Q5; temperature compensation is provided by RT2. The detected and filtered output is also

applied through R28 to the receiver front panel MULT test point.

4-36. MIXER/MULTIPLIER (UHF) A2 (G1).

4-37. The UHF mixer/multiplier module consists of an agc-controlled rf stage, a mixer stage, a local oscillator frequency quadrupler stage, a buffer amplifier stage, an amplifier stage, a feedback amplifier stage and a series regulating stage for gain control. See figure 6-5. The rf input from the antenna is directly coupled to a tap on L10. The input tuned circuit consists of L10 and variable capacitor C30 which is peaked at the incoming rf frequency. The input rf signal is coupled through C31 to gate 1 of the dual gate field effect transistor rf stage Q7. The source of Q7 is supplied through R23 and R24 from the cathode of zener diode VR1.

4-38. The voltage at gate 2 of Q7 is developed by the voltage divider consisting of R28, VR2 and R27 and is supplied to gate 2 of Q7 through R21 and L18. The agc input is connected through R18 to common emitter agc amplifier Q6. The agc input is also connected through L15 and PIN diode CR5 to voltage divider R38 and R39. As the agc voltage level increases with increasing rf signal level, the PIN diode is driven into conduction and thus attenuates incoming signals and prevents Q7 and Q8 from being overdriven. As the agc voltage increases, Q6 is driven harder into conduction and reduces the voltage supplied to gate 2 of Q7 by shunting VR2 and R27 in the voltage divider that provides bias for gate 2 of Q7.

4-39. The output at the drain of Q7 is coupled through C49 to parallel tuned circuit L12 and C35. C35 is adjustable to peak the signal at the received rf frequency. The signal is then coupled through C54 to gate 1 of the dual-gate field effect transistor mixer stage Q8. The quadrupled crystal oscillator frequency is applied to gate 2 of Q8 and the intermediate frequency of 20.6 mhz is produced at the drain of Q8. Variable capacitor C39 is adjusted for maximum if signal output. Impedance matching for the output circuit of Q8 is provided by matching network C38, C39, L13 and C40. Temperature compensation is provided by thermistor RT1 and R45. The if signal is also detected by CR4 and applied through R37 to the receiver front panel major test point MIXER OUT as a positive voltage level.

4-40. The output from the oscillator module is coupled through C1 to the base of quadrupler Q1. Bias for Q1 is supplied through R44 from the voltage divider R1 and R2. C12 is adjusted to peak the signal in the collector of Q1 at four times the frequency applied to the base. The quadrupled frequency is coupled through C16 to the emitter of common base buffer amplifier Q2. C11 is adjusted to peak the signal at the collector of Q2 at four times the oscillator frequency. The signal is coupled through C17 to the base of amplifier Q3. C27 is adjusted to peak the signal at the collector of Q3 at four times the oscillator frequency. The signal is coupled from the collector of Q3 through C23, C36 and L16 to gate 2 of Q8. The voltage at the collector of Q3 is also detected by CR1 and applied through potentiometer R17 to the base of feedback amplifier Q4. The collector voltage of Q4 in turn controls the base to emitter bias for series regulator Q5. Q2 operates between cutoff and saturation. Q5 controls the output of Q2 by controlling the dc supply voltage to Q2 and thus the operating point of Q2. The detected voltage from CR1 is also applied to the front panel major test point MULT.

4-41. MIXER/MULTIPLIER (UHF) A2 (G2).

4-42. The UHF mixer/multiplier module consists of an agc-controlled rf stage, a mixer stage, a local oscillator frequency quadrupler stage, a buffer amplifier stage, an amplifier stage, a feedback amplifier stage and a series regulating stage for gain control. See figure 6-6. The rf input from the antenna is directly coupled to a tap on L10. The input tuned circuit consists of L10 and variable capacitor C30 which is peaked at the incoming rf frequency. The input rf signal is coupled through C31 to gate 1 of the dual gate field effect transistor rf stage Q7. The source of Q7 is supplied through R23 from the cathode of zener diode VR1.

4-43. The voltage at gate 2 of Q7 is developed by the voltage divider consisting of R28, VR2 and R27 and is supplied to gate 2 of Q7 through R21 and L18. The agc input is divided by R18 and R19 and applied to the base of common emitter amplifier stage Q6. The agc input is also connected through L15 and PIN diode CR5 to voltage divider R38 and R39. As the agc voltage level increases with increasing rf signal level, the PIN diode is driven into conduction and thus attenuates incoming signals and prevents Q7 and Q8 from being overdriven. As the agc voltage increases, Q6 is driven harder into conduction and reduces the voltage supplied to gate 2 of Q7 by shunting VR2 and R27 in the voltage divider that provides bias for gate 2 of Q7.

4-44. The output at the drain of Q7 is coupled through C49 to parallel tuned circuit L12 and C35. C35 is adjustable to peak the signal at the received rf frequency. The signal is then coupled through C54 to gate 1 of the dual-gate field effect transistor mixer stage Q8. The quadrupled crystal oscillator frequency is applied to gate 2 of Q8 and the intermediate frequency of 20.6 mhz is produced at the drain of Q8. Variable capacitor C39 is adjusted for maximum if signal output. Impedance matching for the output circuit of Q8 is provided by matching network C38, C39, L13 and C40. Temperature

compensation is provided by thermistor RT1 and R45. The if signal is also detected by CR4 and applied through R37 to the receiver front panel major test point MIXER OUT as a positive voltage level.

4-45. The output from the oscillator module is coupled through C1 to the base of quadrupler Q1. Bias for Q1 is supplied through R44 from the voltage divider R1 and R2. C12 is adjusted to peak the signal in the collector of Q1 at four times the frequency applied to the base. The quadrupled frequency is coupled through C16 to the emitter of common base buffer amplifier Q2. C11 is adjusted to peak the signal at the collector of Q2 at four times the oscillator frequency. The signal is coupled through C17 to the base of amplifier Q3. C27 is adjusted to peak the signal at the collector of Q3 at four times the oscillator frequency. The signal is coupled from the collector of Q3 through C23, C36, and L16 to gate 2 of Q8. The voltage at the collector of Q3 is also detected by CR1 and applied through L9 and potentiometer R17 to the base of feedback amplifier Q4. The collector voltage of Q4 in turn controls the base to emitter bias for series regulator Q5. Q2 operates between cutoff and saturation. Q5 controls the output of Q2 by controlling the dc supply voltage to Q2 and thus the operating point of Q2. The detected voltage from CR1 is also applied to the front panel major test point MULT.

4-46. BUFFER AMPLIFIER A5

4-47. The function of the buffer amplifier is to provide a 50-ohm source impedance for the crystal filter and approximately a 50-ohm load to the mixer/multiplier module. See Figure 6-7. The operating frequency is 20.6 mhz. The module gain is 0 ± 1 db and its 3-db bandwidth is about 4 mhz. The tunable capacitance (C2) is adjusted for maximum gain at 20.6 mhz when J1 is fed from a 50-ohm generator and P1 is loaded with 50 ohms. The +18 vdc supplied to the module is zenered down to about 12 vdc by VR1, a 6.2 volt zener diode. L5 prevents rf from leaving the module on the 18 vdc line and C7 and C8 provide a low ac impedance to keep the signal off the 12 vdc line.

4-48. L1, L2, and C2 are the input matching network. R1 and R2 bias Q1 so that its collector current is about 35 ma. L3 and C5 prevent any residual rf that may be on the 12 vdc line from appearing at the base of Q1. Both R4 and the series combination of R3 and C6 provide degenerative feedback for the amplifier, making it stable and allowing interchangeability of transistors without gain change. L4 is the collector load. C10 accomplishes impedance stepdown from the collector impedance to the 50-ohm impedance of the 7.5 db pad (R5, R6 and R7). R10 suppresses any tendency toward high frequency oscillations. When the signal at the output (P2) is large enough (greater than 0.5 vrms), CR1 rectifies a portion of the signal and C11 filters it to give a dc indication on the condition of the module at the NOISE LIM test point at the front panel of the receiver.

4-49. NOISE LIMITER A5.

4-50. The signal applied to the noise limiter module input J1 flows through an amplifier, a 0.2 μsec delay line and a gating circuit to the output P2 with unity gain. See figure 6-8. The same signal applied to the input also flows into a circuit which establishes a dc voltage directly proportional to the amplitude of the intermediate frequency signal. If a pulse of noise occurs which is from 20 to 30 db higher than the signal voltage, the gate is closed and the output signal is momentarily cut off. A pulse stretching effect occurs in this second loop so that the output signal is gated off for a slightly longer time period than that occupied by the noise pulse. This is to allow complete blanking of the noise pulse. These signal blank out periods are of such short duration that they cause no adverse effect on the audio signal at the receiver output.

4-51. The intermediate frequency input of J1 is applied through an impedance matching network to the base of amplifier stage Q1. C2 and C5 are adjustable to obtain the best impedance match between the 50-ohm input J1 and the amplifier input. Amplifier Q1 boosts the signal level to compensate for signal degradation in delay line DL1 and following circuitry thereby maintaining a net gain of 1 for the module. The signal is coupled from the collector of Q1 to the 0.2 μsec delay line by C8 and C9. C8 and C10 are adjustable for an impedance match with the 50-ohm delay line input impedance. The output of DL1 is applied through a PIN diode gate made up of CR3 and CR4 to module output connector P2. Normally, with no noise pulse present, CR3 and CR4 are forward biased presenting minimum impedance to signal flow to the module output connector P2.

4-52. The signal input at J1 is also applied to the gate control loop consisting of an intermediate frequency amplifier, a detector, an agc feedback loop, a pulse amplifier and a gate driver. Z1 and Z2 are integrated circuit intermediate frequency amplifiers. These amplifiers are broadband tuned as a result of discrete components external to the integrated circuits. Z1 receives an agc input at pin 2. Amplifier stage Q5 is tuned to the intermediate frequency of 20.6 mhz by C38. The collector of Q5 is coupled to the input of integrated circuit Z3 at pin 9. Z3 contains a detector, an agc output, and a pulse amplifier. The agc level is adjusted by R44 and is fed back from Z3 pin 5 to Z1 pin 2. Temperature compensation is provided by CR6, CR7 and CR10.

4-53. The detected signal, along with any noise that might be present, is clamped above ground level through the action of CR8 and applied to the base of emitter follower Q7. The signal from the emitter of Q7 is then applied through R63 and R64 to the base of Q10. However, the signal at the junction of R63 and R64 is clamped below a variable voltage level dependent upon the average peak signal. The AGC from Z3 Pin 5 is also applied through R72 to the base of Q6 allowing C46 to charge up to a value representing the level positive excursion of the detected signal. The base of Q10 is clamped below that level through the action of CR9. When a noise spike occurs extending more positive than the average signal level, it passes through emitter follower Q10 and is amplified by pulse amplifier Q8 and Q9. The noise spike is then coupled through C12 to the base of Q2. The action of CR1, R12, C15, R13, and C14 stretch and couple the pulse to the base of Q3. Q3 cuts off for the duration of the pulse and Q4 goes into conduction applying +12 volts to the cathode of PIN diode gate CR3 via R20 and L5. CR3 and CR4 are then back biased for a time slightly longer than the duration of the noise pulse (+6 volts is applied to the anode of CR4 via R27 and L6) and the noise pulse is effectively removed from the receiver output.

4-54. At the end of the noise blanking pulse, Q3 resumes normal conduction and Q4 is cut off. This effectively connects the cathode of PIN diode gate CR3 to ground via L5, R20, CR2, Q3, and R16 thus supplying forward bias to the PIN diodes opening the gate. The +18 volts on P1-3 is decreased to +6 volts and +12 volts for use within the noise limiter module. The +6 volts is supplied by the regulator circuit consisting of R28, VR1, C26, and R29 and +12 volts is supplied by the regulator circuit consisting of Q11, R33, R34, VR2, and C49. The module signal output is also detected by diode CR5 and applied to receiver front panel major test point NOISE LIM.

4-55. BANDPASS CRYSTAL FILTER FL1.

4-56. The crystal filter type used as FL1 in the receiver is optional. Either one of the following may be used.

4-56A. 50 kHz CHANNEL SPACING BANDPASS CRYSTAL FILTER. This filter is to be used when the channel spacing is 50 kHz. It has a center frequency of 20.6 MHz which establishes the receiver selectivity. Ultimate rejection is 100 dB at 20.6 MHz ± 300 kHz. Rejection is 6 dB or less at 20.6 MHz ± 18 kHz. Insertion loss is 6 dB maximum and ripple across the band at 20.6 MHz ± 15 kHz is 1 dB or less. For the 505564–4 filter, the input impedance is 50-ohms and the output impedance is complex.

4-56B. 25 kHz CHANNEL SPACING BANDPASS CRYSTAL FILTER. This filter is used when the channel spacing is 25 kHz. It has a center frequency of 20.6 MHz which establishes the receiver selectivity. Ultimate rejection is 100 dB at 20.6 MHz ± 300 kHz. Rejection is 6 dB or less at 20.6 MHz ± 10 kHz. Insertion loss is 6 dB maximum and ripple across the band at 20.6 MHz ± 8 kHz is 1 dB or less. For the 505564-3 filter, the input impedance is 50-ohms and the output impedance is complex.

4-57. INTERMEDIATE FREQUENCY AMPLIFIER A6.

4-58. The intermediate frequency amplifier consists of four cascaded common-emitter intermediate frequency stages followed by a detector and a low gain intermediate frequency stage base driven by the fourth stage. See Figure 6-9. The low gain intermediate frequency stage Q5 is an isolation amplifier whose output is coupled through J2 to the 50-ohm output connector J10 on the receiver rear panel. Detector Q6 is biased to perform the detection function and provide an audio signal to the audio preamplifier agc/squelch module. The detector also drives a wideband audio amplifier Q7 and associated circuit components. The first amplifier Q1 is a common-emitter configuration driven by the input intermediate frequency signal through a matching network consisting of C1, C2, C3, and L1. C2 and C3 are provided to adjust the input impedance of the first stage to 50-ohms. The gain of this stage is controlled in a forward agc mode through the base bias resistor R2. The agc voltage controls the base drive through L2 and CR1. R1 and CR2 provide a fixed current to the bias network to maintain a high gain in the transistor in the absence of agc voltage.

4-59. The second and third stages, Q2 and Q3, are identical common-emitter stages driven in cascade by the first stage. The gain of each stage is controlled in a reverse agc mode by the injection of an agc voltage to the emitters of the transistors. The agc voltage is applied to the emitter of Q2 through R12, L9, and CR3. The agc voltage is applied to the emitter of Q3 through R15, L10, and CR4. The fourth stage, Q4, is a common-emitter stage, having no automatic gain control, which drives both the detector and the 50-ohm output isolation amplifier. The isolation amplifier Q5 is a low gain common-emitter stage which drives the 50-ohm output connector through a matching "T" network composed of R23, R24, and R25. The detector stage, Q6, uses its base-emitter junction to rectify the intermediate frequency signal. C38 and C43 and R37 filter out the intermediate frequency signal components and apply the filtered audio to the output connector. C39 couples the audio signal to the wideband audio amplifier which uses Q7 in a common-emitter output stage. The wideband amplifier has a 25 kHz passband.

4-60. PREAMPLIFIER, AF/AGC-SQUELCH A3.

Part No. 8004239G1.

4-61. This module consists of an audio preamplifier,

an automatic gain control amplifier and a squelch circuit. See figure 6-10.

4-62. AUDIO PREAMPLIFIER. The preamplifier consists of an emitter follower input stage, a compressor or audio limiter stage, a common emitter stage, an emitter follower stage driving a low pass filter followed by an active high pass filter utilizing a Darlington combination output amplifier circuit.

4-63. The audio input is coupled by C4 and C18 to the base of emitter follower stage Q9. The squelch input provides bias for Q9 through resistor R50. When the receiver is unsquelched, approximately +15 volts is applied to R50. The other end of R50 is connected to the base of Q9 allowing the preamplifier to operate. When the receiver is squelched, however, the voltage applied to the end of R50 drops to approximately +1 volt, turning off the preamplifier. Emitter resistor R32 is a level control. The signal from the wiper of R32 is applied through R40, R41, and C6 to the base of common-emitter amplifier stage Q13. The junction of R40 and R41 is connected to the audio compression stage Q14 via C5 and R42. The emitter-base dc bias of Q14 depends upon the amplitude of the compressor input.

4-64. The compressor input is an audio signal supplied by the primary of the output transformer of the main audio amplifier in the audio frequency amplifier module. This signal is applied through R45 and C13 to the voltage doubler circuit consisting of CR4, CR5, and C13. C15 is charged up to a positive voltage level that is proportional to the audio amplifier output. With the receiver operating at its rated output, the voltage applied through R44 to the base of Q14 is slightly more negative than the emitter voltage. Q14 is then operating in the cut-off region and maximum impedance to ground is presented to the signal at the junction of R40 and R41. Transistor Q14 is operating in a nonlinear characteristic range due to the very low emitter-to-collector voltage (approximately +16.5 volts at the emitter and +18 volts applied through R43 to the collector). The audio signal at the junction of R40 and R41 is coupled through C5 and R42 to the collector of Q14. The collector voltage swings up and down at an audio rate following the applied audio signal voltage. Since Q14 is now in a cut-off state, maximum impedance is presented to the signal. However, when a relatively high voltage audio signal is detected, C15 is charged up to a correspondingly higher voltage level. This causes a forward bias at the emitter-base junction. A greater change is then produced in the collector current by a given change in collector voltage resulting in a lowered impedance to the audio signal. With Q14 operating in the nonlinear region, the greater the forward emitter-base bias the lower the effective impedance. Therefore the audio signal above the normal audio signal level is limited by the compression stage Q14 before its application to the next preamplifier stage Q13.

4-65. Direct coupling is used between Q13 and Q12. Q12 is an emitter-follower stage having an emitter load consisting of R48, L1, and R36. C11, L1, and C12 make up a pi network low-pass filter. The signal is then coupled to an active high pass filter consisting of Q10, Q11, C7, C8, C9, R36, R37, R38, R30 and R39. The resulting bandpass of the preamplifier is 300 to 3000 hz. Transistors Q10 and Q11 are connected as a Darlington combination amplifier. The preamplifier output is taken from the emitter of Q11 and applied across the receiver front panel AUDIO MAIN ADJ and PHONE ADJ potentiometers. This output is also applied through R51 and C17 to the receiver front panel major test point AF PREAMP.

4-66. AGC AMPLIFIER. The automatic gain control amplifier consists of a differential amplifier, an emitter follower amplifier stage, and two additional amplifier stages. The detected carrier is coupled through R27 to the base of differential amplifier stage Q1. This transistor shares an emitter load network with Q2 consisting of R2, R3, and R5. The operating level of Q2 is adjusted by variable resistor R7. The voltage at the junction of R6 and R9 is regulated by zener diode VR1, R55, RT1 and R10 are for temperature compensation. The adjustable voltage applied to the base of Q2 is established by the voltage divider composed of R6, R7, and R8. Direct coupling is used throughout the agc amplifier. The output from the differential amplifier, the collector of Q2, is applied to the base of emitter follower stage Q8. CR3 is used for temperature compensation. The V_{ec} for the first three transistors is regulated at approximately +12 volts through the action of zener diode VR2 and R11. Emitter follower Q8 output is applied to the base of Q3. The collector of Q3 is connected directly to the base of Q4. The automatic gain control output is taken from the collector of Q4. This output is also applied through R28 to the receiver front panel major test point AGC and to the squelch circuit (located in this same module) via R25 and the receiver front panel squelch controls.

4-67. SQUELCH. The squelch circuit is essentially an electronic switch which turns on the preamplifier when the detected signal reaches a certain level and turns off the preamplifier when the detected signal reaches a lower level. With the receiver front panel SQUELCH switch in the ON position, the agc voltage is applied across R25, the front panel SQUELCH ADJ screwdriver control R1, and R23. The wiper of the front panel control R1 is directly coupled to the base of emitter follower amplifier Q5. Diode CR6 in the emitter circuit of Q5 provides temperature compensation. The emitter of Q6 is maintained at a fixed voltage level by the action of

VR4. In the unsquelched condition, Q5 is cut off and Q6 and Q7 are conducting. If the detected rf level decreases (as indicated by a decrease of the agc level) to the squelch level, the states of these transistors reverse so that Q5 conducts and Q6 and Q7 are cut off. Complete and rapid switching is ensured by the feedback path from the collector of Q7 through R17 to the base of Q6. VR5 and VR6 are used to regulate the positive Q7 emitter voltage.

4-68. The squelch voltage from Q7 collector is connected through R50 to the input of the audio preamplifier. The squelch voltage is also connected via R29 to the receiver front panel major test point SQUELCH. With the receiver front panel SQUELCH control set to the OFF position +18 volts is connected to the front panel control R1. The positive voltage then applied to the base of Q5 will be such that the transistor will be held cut off. Q6 and Q7 will then conduct and a positive voltage will be applied to the preamplifier squelch input enabling it to operate.

4-68A. PREAMPLIFIER, AF/AGC/SQUELCH, A3, ITT PART NO. 8008586G1 (See figure 6-10A)

4-68B. GENERAL. This module replaces and is directly interchangeable with AGC/Squelch module part number 8004239G1. It consists of the same basic functions as the original module including AGC, squelch, compression, audio frequency amplifier and audio frequency filtering. In addition, this module contains improvements for the reduction of unwanted noise associated with carrier attack, squelch release, compression set, squelch attack and squelch quieting. Further, the module provides relief from the annoying and distracting sounds arising from these causes. Additional improvements are a higher ON-OFF squelch ratio, audio frequency compression at any audio output level setting, decreased squelch hysteresis and rejection of pulse noise when the receiver is squelched. (See Figure 6-10A).

4-68C. PREAMPLIFIER, AUDIO FREQUENCY AND SQUELCH CIRCUITS. The audio input comes into P1 through pin 12 and is coupled through C4 to a limiter consisting of diodes CR3, CR4, and CR8. This limiter is used to clip unwanted noise and transient spikes that occur in the audio input. The audio signal is then coupled through the voltage divider network consisting of R31 and R32, through capacitors C5 to the compression control FET Q7. The audio signal is fed through Q7, through capacitor C6 to the audio amplifier Q8. Q8 amplifies the audio signal, coupling the amplified signal through C9 to amplifier Q10. Q10 further amplifies the audio signal and couples the output to a floating limiter consisting of CR6, CR7, R55, C12, and C13. This floating limiter provides limiting action around the d-c bias level and provides further limiting of unwanted noise pulses that occur in the audio passband. At this point in the circuit, the audio is compressed and maintains a near constant peak-to-peak signal level and the floating limiter limits at levels just above and below the compression peak-to-peak audio level. The signal is then coupled through squelch control FET Q11 (described later) to emitter follower Q12. The output from Q12 is then coupled through the low pass filter amplifier circuit consisting of R60, C15, R61, C17, R62, and C16 to operational amplifier U2. The output from the low pass filter network is coupled through C18 to a high pass filter network consisting of C18, C19, R65, R66, C20, R67, R68, Q13, Q14, R69, R70, and R71. The tandem connection of the low pass filter and the high pass filter provides a receiver band pass characteristic that passes 300 to 3000 Hz within +1 to −2 db of the reference frequency of 1000 Hz. The band pass of this filter rolls off the low end to at least 10 db down at 100 Hz and at least 10 db down at 10,000 Hz.

4-68D. AUDIO COMPRESSION CIRCUIT. The audio output from the preamplifier path is coupled back to an amplifier consisting of transistor Q9 and associated biasing components. This stage amplifies the audio, detects and provides a d-c bias to the compression FET Q7. Adjustment of the compression level is accomplished by an adjustment of R41 potentiometer which controls the amount of compression and the signal level output. This feedback compression circuit maintains a constant audio level output with varying audio input signals. The audio output from this module is coupled to the gain control on the front panel; consequently all compression takes place before the main audio gain control, thus compression is obtained at any audio signal level ouptut. The compression detection takes place in diode CR5, and any ripple is filtered out by capacitor C7. This provides d-c bias that is proportional to the audio level to the FET gate through resistors R73 and R34.

4-68E. SQUELCH GATE. FET Q11 provides a series squelch switching action that turns the audio output on and off as a function of the AGC amplifier. When the gate control voltage to Q11 is biased to a turn-off point, no audio signals pass through Q11. The source and the drain voltage potentials are nearly the same, thus providing no d-c level shift when the transistor is turned off. When the transistor is turned on, the audio signal proceeds through Q11 with very little attenuation. It is the equipotential source and drain voltages that provide the quiet switching action of this squelch switch.

4-68F. AGC AMPLIFIER. The automatic gain control amplifier consists of a differential amplifier, an emitter follower amplifier stage and two additional amplifier stages. The detected carrier is coupled through R30 to the base of differential amplifier stage Q1. This transistor shares an emitter load network with Q2 consisting of R2, R3, and R5. The operating level of Q2 is adjusted by variable resistor R7. The voltage at the junction of R6 and R9 is regulated by zener diode VR1. R11, RT1, and R10 are for temperature compensation. The adjustable voltage applied to the base of Q2 is established by the voltage divider composed of R6, R7, and R8. Direct coupling is used

throughout the AGC amplifier. The output from the differential amplifier, the collector of Q2, is applied to the base of emitter follower stage Q3. CR1 is used for temperature compensation. The Vcc for the first three transistors is regulated at approximately +12 volts through the action of zener diode VR2 and R13. Emitter follower Q3 output is applied to the base of Q4. The collector of Q4 is connected directly to the base of Q5. The automatic gain control output is taken from the collector of Q5. This output is also applied through R18 to the receiver front panel major AGC test point, and to the squelch circuit (located in this same module) via R19 and the receiver front panel squelch control potentiometer.

4-68G. SQUELCH. The squelch circuit is essentially an electronic switch which turns on the preamplifier squelch FET when the detected signal reaches a certain level and turns off the FET when the detected signal is reduced to a certain level. With the receiver front panel squelch switch in the on position, the AGC voltage is applied across R19, the front panel squelch screw-driver adjust R1 and R28. The wiper of the front panel control R1 is directly coupled through resistor R23 to pin 3 of the operational amplifier U1. If the detected r-f level increases, the output from operational amplifier pin 6 goes positive and turns on the squelch FET Q11 in the preamplifier circuitry. If the detector r-f level decreases, (as indicated by a decrease of the AGC level) to the squelch level, the output from operational amplifier U1 decreases thus turning off the squelch FET Q11 in the pre-amplifier circuitry. Complete and rapid switching is insured by the feedback path resistor R22 around the operational amplifier U1. Diode CR2 provides fast decay of the squelch switch filtering capacitor C14 when the squelch switch turns off. When the receiver unsquelches, resistor R24 provides a short time constant action to charge C14 so that a small squelch delay occurs to provide inhibiting of any unwanted transients at the time of initial detection of input signals. Transistor Q6 provides a monitor output drive and serves as an isolation transistor for the squelch test point.

4-69. AUDIO FREQUENCY AMPLIFIER A4.

4-70. The audio frequency amplifier consists of two separate audio amplifier systems. The main audio amplifier receives an input signal controlled by the AUDIO MAIN ADJ screwdriver adjustment on the receiver front panel and supplies an output to a connector on the receiver rear apron for remote speaker operation. The secondary audio amplifier receives an input controlled by the PHONE ADJ control on the receiver front panel and supplies an output to the PHONE OUTPUT jack on the receiver front panel. See figure 6-11.

4-71. MAIN AUDIO AMPLIFIER. The main audio amplifier consists of a common-emitter amplifier stage, a phase-splitter stage, a push-pull driver stage, a push-pull output stage and an output transformer. The input audio signal is coupled through C1 and R16 to the base of common-emitter amplifier stage Q5. Degenerative feedback to this stage is employed to provide adequate regulation of the output signal voltage. This negative feedback signal is derived from output stage Q3 and is also coupled to the base of Q5 via R24 and C11. The signal from the collector of Q5 is coupled through C2 to the base of phase splitter Q6. The phase splitter provides signals of equal magnitude and opposite polarity to the output driver stage consisting of Q1 and Q2. Temperature compensation of bias for the driver stage is provided by CR2 and CR3.

4-72. The output signal from the emitters of driver stage Q1 and Q2 is direct coupled to the push-pull output stage at the base of Q3 and Q4. The collectors of Q3 and Q4 are connected to the primary of output transformer T1. The center tapped secondary of T1 is connected to a rear apron connector on the receiver. Signal voltage across T1 is limited to approximately 43 volts peak-to-peak maximum by the action of zener diodes VR1 and VR2. A compression output to the audio preamplifier/agc squelch module is provided from the collector of Q3. The signal from the collector of Q4 is divided by R46 and R47 and coupled through C24 to the receiver front panel major test point MAIN AF.

4-73. SECONDARY AUDIO AMPLIFIER. The secondary audio amplifier consists of a common-emitter amplifier stage, a phase splitter, a push-pull output stage and an output transformer. The input audio signal is coupled through R25 and C13 to the base of common-emitter amplifier stage Q7. Degenerative feedback from the collector of Q9 is also coupled to the base of Q7 via C14 and R26. The signal is coupled from the collector of Q7 through C19 to the base of phase splitter stage Q8. High frequencies are attenuated through the action of C20 and R37. Q8 provides signals of equal magnitude and opposite polarity to the push-pull output stage consisting of Q9 and Q10. The push-pull output stage drives the output transformer T2. The voltage across the primary of T2 is limited to a maximum of approximately 43 volts peak-to-peak by the action of zener diodes VR3 and VR4.

4-74. SURGE PROTECTION. Surge protectors are provided to protect the audio amplifier output circuits from ± 1000 volts peak input pulses applied to each audio output. Protection for the main audio amplifier output is provided by surge protectors E1 and E2. These are mounted on terminal board TB1 adjacent to the rear apron connector J2. Protection for the secondary audio amplifier is provided by E8 mounted on the back of the receiver front panel PHONE OUTPUT jack.

4-75. POWER SUPPLY PS1.

4-76. The power supply consists of a power transformer, a bridge rectifier, a voltage regulating circuit, a battery charging circuit, and a short-circuit protection circuit. See figure 6-12. The power supply is designed to operate from either ac or dc voltages. Jumpers are provided on terminal board TB1 to allow the power supply to operate at any one of the following primary voltages: 105, 120, 210 or 240 vac ± 10%. Usable frequency for primary ac power is 47 to 420 hz. In case of ac power failure, primary power is supplied to the power supply from an external battery. With the supply operating on ac, voltage is applied to the primary of transformer T1 via TB1. The secondary of T1 connects to the bridge rectifier CR1, CR2, CR3, and CR4. An unregulated output of approximately +30 volts is provided at the junction of CR1 and CR2 for use as crystal oven heater power for the oscillator module. This same output flows through R2 and is reduced to +18 volts ± 0.5% by series-pass transistor Q3 to supply the regulated voltage required by the receiver.

4-77. REGULATOR CIRCUIT. Q6 and Q7 form a differential amplifier driving emitter resistor R15. The regulator output voltage is applied across voltage divider R16, R17, and R18. A sample of the output, from potentiometer R17, is applied to the base of Q7. The level of the output voltage may be set by adjusting R17. A reference voltage established by zener diode VR2 is applied to the base of Q6 which is the other differential amplifier input. The output of the collector of Q7 is directly coupled to the base of common-emitter amplifier stage Q5. The voltage at the emitter of Q5 is held at a constant value by VR1. A second input to the base of Q5 is applied by the short-circuit protection circuit via CR5. When the supply is operating with no short-circuit present, CR5 will be back biased effectively disconnecting the short-circuit protection input from the base of Q5.

4-78. The output of amplifier stage Q5, at the junction of resistors R9 and R6, is direct coupled to the base of common-emitter amplifier stage Q2. The collector of Q2 is direct coupled to the base of series-pass transistor Q3. The amplitude and polarity of this signal is such that of this signal is such that a regulated +18 volts is produced at the emitter of Q3. Special circuitry is necessary to facilitate the start-up of the regulator. When power is turned on, capacitor C3 is charged up through resistor R7. The junction of R7 and C3 is connected to the base of Q5 through R8. When the voltage applied to the base of Q5 becomes enough positive it overcomes the positive emitter voltage established by VR1 and Q5 begins to conduct through R9 and R6. Current through R6 causes Q2 to start conduction which, in turn, allows conduction through series pass transistor Q3. When sufficient current flows on the regulated +18 volt line, the normal regulator takes control and the output is maintained at +18 volts. The relatively large value of R8 sufficiently isolates the start-up circuit to allow Q5 to be controlled by the differential amplifier Q6 and Q7 when these transistors receive adequate operating voltage.

4-79. BATTERY CHARGING CIRCUIT. The battery is charged by a 300 ma nominal constant-current source when the power supply is operating from ac. The battery charge path is from the junction of CR1 and CR2 through R22 and R23, Q8 and CR9 to the battery bus. Q8 is the series-pass transistor in the charging circuit. A constant voltage is applied to the base of Q8. This constant voltage is established by the voltage dropped across forward-biased diode string CR6, CR7, and CR8 (approximately 2 volts is dropped across the diodes). The charging current through emitter resistors R22 and R23 determines the emitter-base bias in Q8 and maintains the 300 ma nominal trickle charge rate. Reverse battery polarity protection is provided by stage Q9. With proper battery polarity, Q9 is in the cut-off region. However, if the battery is connected backward, a negative voltage will be applied to the base of Q9 causing heavy conduction. This eliminates the 2 volts dropped across the three diodes CR6, CR7 and CR8 and applies a back emitter-base bias to series pass transistor Q8. Transistor Q8 is then driven into the cut-off region and the battery charge path is interrupted.

4-80. SHORT CIRCUIT PROTECTION. When a short circuit occurs, a heavy current tends to flow through R2, in series with the series pass transistor Q3. An increase in current flow also occurs in R1 and R3. A forward emitter-base bias for Q1 is developed across R1 and Q1 starts to conduct. This applies forward bias to the emitter-base junction of Q4 which begins to conduct through R5. The collector of Q4 is connected through CR5 to the base of Q5 driving it into cutoff. Q5 is an amplifier stage in the regulator circuitry discussed in a previous paragraph. As a result of the regulator action, series pass transistor Q3 is cut off thus removing the power supply regulated output from the receiver modules. C2 across the emitter-base junction of Q1 prevents extraneous activation of the short-circuit protection as a result of momentary changes in load. The short-circuit protection circuit is latching and once triggered by an overload, the regulated output is not reapplied until the receiver is turned off and then on again. Once an overload has occurred, current flows through Q4, R5 and R1. Current through R1 holds Q1 conducting which in turn maintains a forward bias on Q4 and holds it in conduction and primary power has been removed from the power supply.

4-81. AC POWER FAILURE. In case of ac power failure, primary power will be supplied from the battery. Current flow will be from the battery bus through isolation diode CR10, R2 and series pass transistor Q3 to all receiver modules requiring regulated voltage. The same regulator circuit is used regardless of whether using an ac or a dc power source.

CHAPTER 5

MAINTENANCE

5-1. INTRODUCTION. This chapter contains information and instructions for maintenance personnel to accomplish satisfactory operation of the receivers. It contains organizational/field maintenance and includes fault isolation, corrective maintenance, and a performance test procedure.

ORGANIZATIONAL/FIELD MAINTENANCE

5-2. GENERAL.

5-3. This section contains information necessary for maintenance of the UHF receiver and the VHF receiver at the organizational/field level.

5-4. Table 5-1 contains a listing of maintenance test equipment and special tools required for maintenance of the receivers.

Table 5-1. Maintenance Test Equipment and Special Tools

TEST EQUIPMENT	CHARACTERISTIC
Multimeter, Simpson Model 360	Dc voltage 0 to 5000 in 7 ranges Ac voltage 0 to 5000 in 6 ranges Dc current 0 to 10 amperes in 6 ranges Dc resistance 0 to 20 megohms in 3 ranges -20 to +50 db in 4 ranges Accuracy ±3% full scale dc ±5% full scale ac
Signal Generator, HP608C/D	10 mhz to 180 mhz in 5 bands
Frequency Counter, (HP5245L and HP5253B)	Measures frequencies and repetition rates from 0 to 50 million ppx. Converter subtracts multiples of 10, 50, or 200 mhz from cw frequency to be measured providing the difference to be measured to the counter.

Table 5-1. Maintenance Test Equipment and Special Tools (Cont.)

TEST EQUIPMENT	CHARACTERISTIC
Oscillator, Audio Hewlett Packard 200 AB	Frequency Range: 20 hz to 40 khz; 4 bands, ±2% calibration accuracy; 1 watt output, 60 ohms at 24 volts. Maximum distortion 1% from 20 hz to 20 khz; 2% from 20 khz to 40 khz.
Oscilloscope Tektronix Model 515A	Vertical: Frequency response: dc to 15 mhz ac 2 hz to 15 mhz Input impedance: 1 megohm, 30 $\mu\mu$f; With P410 probe: 10 megohm, 10.5 $\mu\mu$f Horizontal: Time base: from 0.2 μsec/cm to 2 sec/cm. Frequency response dc to 50 khz, 5 db
Cable Extension Kit ITT P/N 8004810G1	

5-5. FAULT DIAGNOSIS.

5-6. Prior to starting actual diagnosis of faults perform the following:

a. Plug the headphones into the AUDIO OUTPUT jack on the front panel, and observe receiver performance on known signals.

b. Adjust the AUDIO PHONE ADJ gain control for a desired level. Disable the squelch if desired.

NOTE

Since the phone audio channel is separate from the main audio channel, faults in the main audio channel may not be observed by this method. It is also possible that unknown faults in the phone audio channel may be present.

c. Compare the audio heard with the audio that is expected.

d. Confirm, if possible, that the fault actually exists.

e. Based on these initial observations such as distorted audio, degraded sensitivity, etc. refer to table 5-2 for a most probable cause of the fault.

5-7. TEST POINT INDICATIONS. Perform the following checks and observation at the test points specified. Compare the observed results with the required results shown in table 5-3.

a. Always verify that receiver B+ is normal, by checking UNREG B+ and REG B+ test points.

b. Always verify that injection into the mixer is normal by checking the MULT test point.

c. Check that signals are being received by observing the AGC test point.

d. Check that signals are present in the main audio channel by observing the MAIN AF test point.

5-8. With the observations made in paragraph 5-5 steps a through e. complete the diagnosis of the fault to the module level test point measurements. Compare the observed results with the required results shown in table 5-3. Based on the test point observations, diagnose the module which is the cause of the observed fault or deficiency by referring to table 5-4.

5-9. The following procedures should be adhered to for expeditious fault analysis and repair.

a. When a test point appears to have an incorrect indication, verify that the VTVM is on the correct scale, and that the input signal levels are as expected.

b. When a test point reading leads to some conclusion regarding the module which is faulty, verify all other related test point readings which would support that conclusion.

c. Do not make adjustments to the receiver with undiagnosed faults present in the receiver, except as follows:

1. Set AUDIO MAIN ADJ output level as desired.
2. Set AUDIO PHONE ADJ output level as desired.
3. Set SQUELCH to ON or OFF as desired.

d. When agc performance, squelch threshold, audio output level or sensitivity show a significant degradation, do not attempt to restore normal condition through adjustment. (While such adjustment might seem correct or improve a condition noted, it will only mask the original symptoms, and make further diagnosis difficult.)

e. Do not swing tuning controls through their range in and attempt to see if they respond.

f. Do not swing tuning controls through their range if they have been misadjusted.

g. Perform only those retuning and alignment adjustments indicated, and then only in connection with service restoration following replacement of a faulty module.

h. Do not adjust the power supply. Adjustment to this module shall be made at Special Maintenance Level.

5-10. ADDITIONAL DIAGNOSTIC PROCEDURES. In the event an observed fault is not corrected by replacement of the module indicated in tables 5-2, 5-3, or 5-4, further diagnostic procedures will be required and should be performed as indicated in paragraphs 5-11 through 5-18.

Table 5-2. Receiver Fault Isolation Indications

STEP	SYMPTOM	PROBABLE CAUSE
1	No signal, only background noise	Oscillator; oscillator synthesizer; mixer/multiplier
2	Degraded sensitivity, high background noise	Oscillator; oscillator synthesizer; mixer multiplier
3	Degraded sensitivity, medium background noise	Noise Limiter; if amplifier
4	Degraded sensitivity, low background noise	IF amplifier; agc/squelch
5	No signal, no noise	Power supply; audio amplifier; agc/squelch
6	High impulse noise level (static)	Noise limiter
7	Distorted audio	Audio amplifier; agc/squelch; if amplifier
8	AC hum in audio	Power supply
9	Excessively high audio, with distortion	Agc/squelch audio amplifier
10	No main af output, phone	Audio amplifier; agc/squelch
11	No phone audio output; Main af output OK	Audio amplifier; agc/squelch
12	Receiver off frequency; LO OK; oven OK	Crystal
13	Receiver off frequency; LO low; oven OK	Oscillator; oscillator-synthesizer
14	Receiver off frequency; LO OK; oven high/low	Oscillator; oscillator-synthesizer

Table 5-3. Normal Front Panel Test Point Indications

STEP	TEST POINT	FUNCTION	SIGNAL INPUT	INDICATION	COMMENTS
1	UNREG B+	Measures output voltage of power supply full wave rectifier.	Any	a. 27 vdc to 40 vdc	When primary power is ac. Voltage varies with line voltage.
				b. 21.5 vdc to 29.5 vdc	When primary power is a 24 volt battery.
2	REG B+	Measures output voltage of power supply regulator	Any	17.90 to 18.10	This voltage is set with a voltmeter more accurate than is commonly found at the installation. Do not reset in the field. If the meter in the field has an accuracy of ± 2 percent of full scale on a 30 volt scale the B+ should be regarded as correct if it reads 17.4 volts to 18.6 volts.
3	AGC	Measures output voltage on agc bus	a. No signal (SQUELCH switch OFF)	2.6 vdc to 3.2 vdc	
			b. No signal (SQUELCH switch ON)	1.5 vdc to 2.5 vdc	
			c. −102 dbm (SQUELCH Switch OFF)	5 vdc minimum	
			d. 0 dbm	9 vdc to 10 vdc	
4	SQUELCH	Measures squelch control voltage	a. No signal (SQUELCH switch OFF)	14 vdc to 16 vdc 7 vdc to 9 vdc	P/N 8004239G1 P/N 8008586G1
			b. No signal (SQUELCH switch ON)	less than 1 vdc	

Table 5-3. Normal Front Panel Test Point Indications (Cont)

STEP	TEST POINT	FUNCTION	SIGNAL INPUT	INDICATION	COMMENTS
			NOTE		
			Unless otherwise specified SQUELCH switch should be in OFF position.		
5	IF.	Measures ac and dc voltage at output of detector stage.	a. No signal	2.5 vdc to 4.0 vdc	
			b. Any level from −97 dbm to +13 dbm	3.0 vdc to 5.0 vdc	As the generator power level is increased from −120 dbm to −97 dbm this voltage will rise to some value within the indicated range. From −97 dbm to +12 dbm the voltage will be almost constant, increasing only about 0.1 volt.
			c. −97 dbm to +12 dbm modulated 30 percent at 1 khz	50 mvac to 300 mvac	
6	LO	Measures rectified rf output of oscillator module	Any	0.25 vdc to 0.8 vdc*	
7	MULT	Measures rectified rf output of multiplier	Any		
			a. VHF	0.95 vdc to 1.07 vdc (See Table 3-5 for exact level)	Exact level is set during tuning. With LEVEL ADJ potentiometer maximum clockwise during tuning indicator will be 1.3 V to 2.0 v.

* With external generator input (crystal removed) there will be no reading with G3 oscillator.

Table 5-3. Normal Front Panel Test Point Indications (Cont)

STEP	TEST POINT	FUNCTION	SIGNAL INPUT	INDICATION	COMMENTS
			b. UHF	2.0 vdc to 4.0 vdc (See Table 3-3 for exact level)	Exact level is set during tuning. With LEVEL ADJ potentiometer maximum clockwise during tuning, indicator will be 5.5 V to 20 V.
8 (a)	LO. OVEN (G1, G2)	Measures oscillator oven heater voltage	Any	See Comments	Connect positive terminal of voltmeter to UNREG B+ and negative terminal to LO. OVEN. The observed indication will be the voltage across the heating element (26 ohms). This voltage may go as high as about 25 volts (25 watts of power dissipated in heating element) when the unit is calling for the maximum heat to as low as zero volts (zero watts) when calling for no heat. In a normal unit the average power dissipated in the heating element will depend on the ambient temperature. The power level may cycle between two levels. The cycle time may be 5 minutes or longer.

CAUTION

A grounded case voltmeter shall not be used to measure L.O. oven voltage. Use of this type voltmeter may cause damage to the crystal controlled oscillator (A1).

Table 5-3. Normal Front Panel Test Point Indications (Cont)

STEP	TEST POINT	FUNCTION	SIGNAL INPUT	INDICATION	COMMENTS
(b)	LO. OVEN (G3)	Measures voltage across resistor in series with oscillator oven heater.	Any	See Comments	Connect positive terminal of voltmeter to UNREG B+ and negative terminal to LO OVEN. The observed indication will be a voltage across the metering resistor of .499 ohms. This voltage at initial equipment turn on will be .4 ± .1 volt and indicates maximum heat demand by the oven. With minimum heat demand the reading will be .1 ± .05 volts. The metering voltage may be zero in very high ambient temperature.

Table 5-3. Normal Front Panel Test Point Indications (Cont)

STEP	TEST POINT	FUNCTION	SIGNAL INPUT	INDICATION	COMMENTS
9	MIXER OUT (UHF and VHF)	Measures rectified if voltage at output of mixer	+10 dbm (See comments)	0.2 vdc or greater	Adjust the generator frequency slightly off-channel for maximum indication. (This disables the agc and permits a usable indication).
10	NOISE LIM (This monitors equivalent test point in buffer amplifier)	Measures rectified if voltage at output of limiter.	+10 dbm (See comments)	0.2 vdc or greater	Adjust the generator frequency slightly off-channel for maximum indication. (This disables the agc and permits a usable indication).
11	AF PRE-AMP	Measures ac voltage at output of af preamplifier.	−97.5 dbm to +13 dbm, 30 percent modulation at 1 khz. AUDIO MAIN ADJ potentiometer maximum counterclockwise.	0.3 vac to 1.0 vac typical	Actual level varies with setting of R32 on AGC/squelch module.
12	MAIN AF	Measures sample of ac voltage at output of main audio amplifier	−97.5 dbm to +13 dbm, 30 percent modulation at 1 khz AUDIO MAIN ADJ potentiometer maximum clockwise.	1.5 vac to 2.5 vac	

Table 5-4. Abnormal Test Point Indications

REG B+	AGC	SQUELCH	IF	LO	MULT	MIXER OUT	NOISE LIM	AF PREAMP	MAIN AF	HEAD PHONES	PROBABLE CAUSE
Low											Power supply
High											Power supply
OK	Low			Low							Oscillator
OK	Low			OK	Low						Mixer/multiplier
OK	Low				OK	Low					Mixer/multiplier
OK	Low				OK	High	Low				Noise limiter
OK	Low		OK		OK	High	High	Low			IF
OK	Low		Low		OK	High	High	Low			IF
OK	Low		High		OK	High	High	High		Distortion	Agc/squelch
OK	High		Low		OK			Low			Agc/squelch
OK	OK	Low			OK			Low			Agc/squelch
OK	OK	OK	OK		OK			Low			Agc/squelch
OK	OK				OK			OK	Low		Audio amplifier
OK	OK				OK				OK	Static	Noise limiter
OK	OK				OK				OK	Hum	Power supply

5-11. POWER SUPPLY. When fault diagnosis indicates that a fault exists in the power supply module, and replacement of the module does not correct the fault refer to table 5-5.

5-12. RF CIRCUITS. When fault diagnosis indicates a loss of sensitivity in the mixer/multiplier module as shown by abnormally low test point readings of the mixer output, and the LO injection into the mixer is normal as indicated by a normal MULT test point reading, and replacement of the mixer multiplier modules does not correct the condition, refer to table 5-6.

5-13. NOISE LIMITER OR BUFFER AMPLIFIER. When initial fault diagnosis indicates that a fault exists in the noise limiter involving the noise limiter through path signal, as shown by high MIXER OUT and low NOISE LIM test point readings, and replacement of the module does not correct the fault, the fault may be a shorted signal path in a component following the noise limiter. Disconnect the coaxial cable at the output of the noise limiter. If the noise limiter test point now indicates a reading equal to or somewhat higher than its normal value for agc disabled conditions, reconnect the coaxial cable: refer to table 5-7.

5-14. IF AND CRYSTAL FILTER. When fault diagnosis indicates that a fault exists in the if amplifier module involving sensitivity, and module replacement does not correct the fault, refer to table 5-8.

5-15. AGC. When fault diagnosis indicates that agc is very low, and not responsive to high signal levels, with excessively high test point readings at MIXER OUT and NOISE LIM together with receiver overload and distorted audio, and replacement of the agc/squelch module does not correct the fault, the fault may be a shorted agc buss in an external module. Replace the if amplifier module. If this does not correct the faulty condition replace the mixer/multiplier module. If this does not correct the condition, check for a possible agc buss wire short. If agc voltage, as read at the AGC test point, is abnormally high but other test point readings indicate excessive signal, overload and distortion, the fault may be an open agc buss wire to the if amplifier and/or mixer/multiplier module.

5-16. AUDIO CIRCUITS. Most of the probable faults in the audio system will be in the af amplifier, or the agc/squelch modules. This includes loss or degradation of audio in either main or phone outputs, or excessive audio together with distortion or high audio levels due to a fault in the audio compression circuits. If replacement of the module indicated as the most probable cause does not correct the fault, replace the other module. If the fault is still present, refer to paragraph 5-18.

5-17. WIDE-BAND DATA OUTPUT AND IF OUTPUT FUNCTIONS. Failures of the wide-band data output and if output functions of the receiver (when all other receiver functions are normal) are caused only by the if amplifier or external wiring.

5-18. INTERCONNECTING WIRING. The failures contributed by broken or shorted wires are negligible. However, if fault diagnosis by means of the procedures in the preceding paragraphs is not successful, and a discontinuity or short in chassis wiring is suspected, disconnect the effected modules as required, and make the necessary continuity and short tests utilizing the applicable circuit diagrams.

5-19. MODULE REMOVAL AND REPLACEMENT. See figure 5-1.

NOTE

Observe that POWER ON-OFF switch is in the OFF position and disconnect ac power connector at rear of chassis.

NOTE

When any reference is made to the oscillator module in the module removal and replacement procedures, the same information applies to the oscillator-synthesizer and oscillator-multiplier as these three modules are mechanically and electrically interchangeable.

5-20. TOP COVER. To remove the top cover from either the UHF receiver or the VHF receiver, loosen the six captive 6-32 flat head Phillips head retaining screws. Replacement is the reverse of removal. Push top edges of cover down to avoid rf interference.

CAUTION

When disconnecting and replacing coaxial cables from modules, use two 1/4 inch open-end wrenches. Do not apply excessive pressure to connectors when reconnecting to module.

5-21. TUNABLE FILTER. (UHF, 8004242G1) (VHF, 8004243G1) To remove the tunable filter from the UHF receiver or the VHF receiver, disconnect the two cables using two 1/4 inch open-end wrenches. Loosen the captive 6-32 Phillips head screw holding the filter to the bottom of chassis and the two 8-32 Phillips head screws from the right side panel. The 8-32 side panel screw, toward the front, is best engaged through the front panel door. The tunable filter module can then be lifted directly upward. Replacement is the reverse of removal.

5-22. ANTENNA COUPLER (UHF, 8004747G1) (VHF 8004503G1) The antenna coupler is mounted to the inside of the receiver rear apron. To remove the antenna coupler from the UHF receiver or the VHF receiver, disconnect the coaxial cable or terminator from the type N connector of the antenna coupler which extends through the receiver rear apron toward the back.

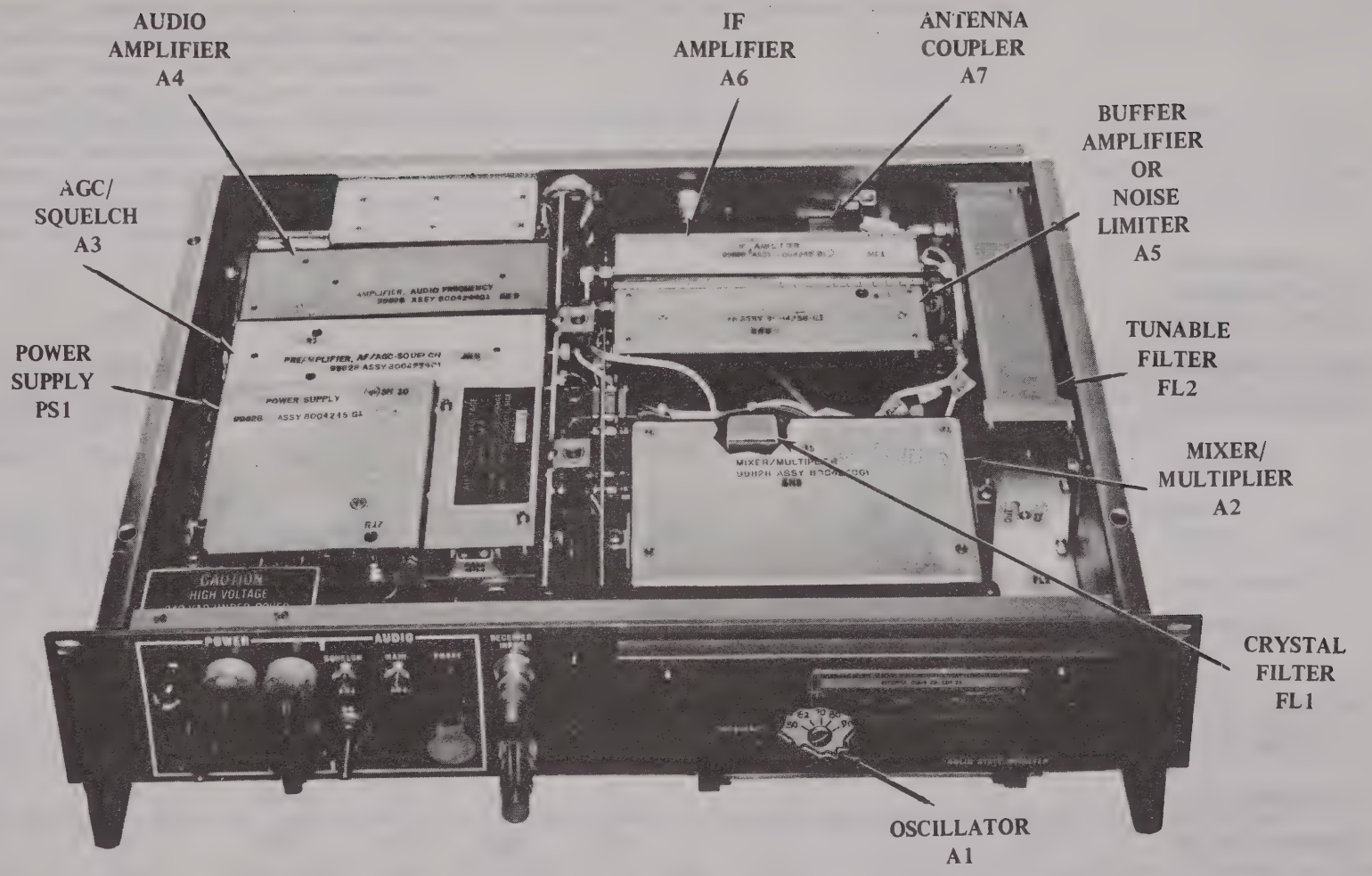


Figure 5-1. Module Location and Identification

Table 5-5. Power Supply Fault Analysis

TYPE OPERATION	REG B+	UNREG B+	AC ON LIGHT	BLOWN FUSE LIGHT	AC VOLTAGE AT FUSES	AC LINE VOLTAGE ON INPUT CABLE	BATTERY VOLTAGE	BATTERY TERMINAL VOLTAGE	PROBABLE CAUSE
AC Operation Only	Low	Low	On	Off	Low				Low AC line voltage
AC Operation Only	Low	Low	Off	Off	Low				Low AC line voltage
AC Operation Only	Zero	Zero	Off	On					AC line fuse (2)
AC Operation Only	Zero	Zero	Off	Off	OK (1)				Power On-Off Switch
AC Operation Only	Zero	Zero	Off	Off	Zero	OK (3)			Ac line filter
AC Operation Only	OK	OK						Low (5)	Power Supply (7)
Battery Operation Only	Zero	Zero					OK (4)		Power On-Off Switch
Battery Operation Only	Zero	Zero					Zero	OK (5)	DC line filter
Battery Operation Only	Low	Low					Low		Low battery voltage
AC and Battery	Low	Low			Low		Low		Both inputs low (7)
AC or Battery	Zero	OK							Short on Reg B+ distribution bus, in some module. (6)

Notes:

(1) AC line voltage may be measured at the fuseholders with caps and fuses removed; however if other equipments in the installation are served by the same AC line and the basic line voltage is known to be correct, a quick check for the presence of AC voltage may be made by removing one of the fuses and reinstalling the fuse cap. Its indicating light will illuminate if AC voltage is present and the other fuse is intact.

(2) If a fuse is blown it is likely that the power supply module which was in use has an internal fault.

(3) Measured on AC input cable disconnected from rear of chassis.

(4) Measured on battery input filter at inside rear of chassis.

(5) Measured on battery terminals of main cable disconnected from rear of chassis.

(6) With short on Reg B+ distribution line in some external module, power supply goes into "Overcurrent protection" mode and will remain there indefinitely until short is cleared and regulator is reset by turning power off for approximately 20 seconds, then turning power on. Disconnect modules, one at a time, with power off at least 20 seconds, until the short is cleared and Reg B+ returns to normal. Replace the indicated module.

(7) The receiver normally supplies a nominal 300 ma trickle charge to a low battery. If a good, but discharged battery is not recharged a fault probably exists in the power supply.

Table 5-6. RF Circuits Fault Analysis

STEP	PROCEDURE	COAXIAL ADAPTER REQUIRED	MIXER OUTPUT TEST POINT READING (NOTE 2)	FURTHER DIAGNOSIS REQUIRED	PROBABLE CAUSE
1	Bypass the antenna jack and the front-panel coaxial link, by connecting antenna or signal source directly to the receiver input at the front panel.	Type N to type BNC	OK	None	Antenna jack, or cable from antenna jack, to coax link, or coax link.
			Low	Proceed to step 2.	
2	Bypass the antenna coupler by connecting antenna or signal source directly to tunable filter input.	Type N to UG 1464	OK	None	Antenna coupler, or cable from front panel to antenna coupler.
			Low	Proceed to step 3.	
3	Bypass the tunable filter by connecting antenna or signal source directly to mixer RF input.	Type N to UG 1465	High (Note 1)	None	Tunable filter.
			Low	See para 5-18	

Notes:

(1) The tunable filter normally has approximately 5 db insertion loss at its center frequency. Bypassing the tunable filter in a normal receiver will result in a higher-than-normal reading at the mixer output test point.

(2) Mixer output test point reading has compared with the value given in Table 5-3 with signal source slightly off frequency thereby disabling agc.

Table 5-7. Noise Limiter/Buffer Amplifier Output Fault Analysis

STEP	PROCEDURE	TEST POINT READINGS	FURTHER DIAGNOSIS REQUIRED	PROBABLE CAUSE
1	Signal input at +10 dbm; all signal path connections made; signal generator frequency slightly off channel for agc is disabled.	Mixer high; Noise Limiter low.	Proceed to step 2.	
2	Disconnect signal cable input to if amplifier	All normal for this condition	None	IF amplifier
		Unchanged	Proceed to step 3.	
3	Disconnect crystal filter output cable	All normal for this condition	None	Cable
		Unchanged	Proceed to step 4.	
4	Disconnect crystal filter input cable	All normal for this condition	None	Crystal filter
		Unchanged	Proceed to step 5.	
5	Disconnect cable from output of noise limiter module	All normal for this condition	None	Cable

Table 5-8. IF and Crystal Filter Fault Analysis

STEP	PROCEDURE	TEST POINT READING	FURTHER DIAGNOSIS REQUIRED	PROBABLE CAUSE
1	Signal input at +10 dbm; receiver in normal configuration.	agc (less than 9.0 volts) if low or normal;	Proceed to step 2.	
2	Bypass the crystal filter with another crystal filter.	All normal	None	Crystal filters
		Unchanged	Proceed to step 3.	
3	Bypass crystal filter by connecting the output of the noise limiter directly to the input of the if amplifier.	All normal	None	Coaxial cable between noise limiter and crystal filter, or between crystal filter and if amplifier.
		Unchanged	See para 5-18.	

Disconnect the one cable from the tunable filter and the remaining cable from the antenna coupler, using two 1/4-inch open-end wrenches. Loosen the four 4-40 pan head Phillips head mounting screws holding the antenna coupler to the rear panel. Loosen one captive 8-32 Phillips head screw at the right end of the if amplifier module, slide to right, and lift out antenna coupler. Replacement is the reverse of removal.

5-23. MIXER/MULTIPLIER AND CRYSTAL CONTROLLED OSCILLATOR. The mixer/multiplier module is mounted to the top of the crystal controlled oscillator. Therefore, the mixer/multiplier can be removed alone by following the procedure in the following paragraph. The crystal controlled oscillator however, cannot be removed without first removing the mixer/multiplier module. The two modules may also be removed together as a unit from the chassis.

5-24. MIXER/MULTIPLIER (UHF, 8004240G1) (VHF 8004241G1) To remove the mixer/muliplier module disconnect the three coaxial cables, using two 1/4-inch open-end wrenches, and the connector at J7 by loosening the two captive 4-40 screws on the plug. Loosen the two 8-32 captive Phillips head screws at the ends of the module, holding it down to the module beneath. Replacement is the reverse of removal.

5-25. CRYSTAL CONTROLLED OSCILLATOR. To remove the crystal controlled oscillator from either the UHF receiver or the VHF receiver, remove the mixer/multiplier module by following the procedure in the preceding paragraph. Remove connector at J6 by loosening two captive 4-40 screws on the plug. Loosen the four captive 8-32 Phillips head screws (holding the module in place) to the bottom of the chassis. Replacement is the reverse of removal.

5-26. BANDPASS CRYSTAL FILTER. To remove the bandpass crystal filter disconnect the two coaxial cables using two 1/4-inch open-end wrenches. Loosen the four 6-32 Phillips head screws through the module side flanges into the chassis bottom. Loosen the 8-32 Phillips head screw at the right end of module. Slide the module to the right until the alignment pins on the left end of the module clear the nylon bushings in the center partition of the chassis. Then remove the module by lifting directly upward. Replacement is the reverse of removal.

5-27. NOISE LIMITER. To remove the noise limiter or buffer amplifier from the UHF receiver or the VHF receiver, disconnect coaxial cable using two 1/4-inch open-end wrenches and loosen one captive 8-32 Phillips head screw at the right end of module. Disconnect the remaining cable from the crystal filter. Slide the module to the right until the alignment pins clear the nylon bushings in the center chassis partition and lift directly upward. Replacement is the reverse of removal.

5-28. INTERMEDIATE FREQUENCY AMPLIFIER. To remove the if amplifier from the UHF receiver or the VHF receiver, disconnect the two coax cables using two 1/4-inch open-end wrenches and loosen one captive 8-32 Phillips head screw at the right end of the module. Slide the module to the right until the alignment pins clear the nylon bushings in the center chassis partition and lift directly upward. Replacement is the reverse of removal.

5-29. POWER SUPPLY. To remove the power supply from the UHF receiver or the VHF receiver loosen the two captive 8-32 Phillips head screws at the left end of the module. Slide the power supply module to the left until the alignment pins clear the nylon bushings in the center chassis partition and lift, directly upward. Replacement is the reverse of removal.

5-30. AGC/SQUELCH. To remove the agc/squelch module, loosen the captive 6-32 Phillips head screw at the left end of the module. Slide the agc/squelch module to the left until the alignment pins clear the nylon bushings in the center chassis partition and lift directly upward. Replacement is the reverse of removal.

5-31. AUDIO AMPLIFIER. To remove the audio amplifier module, loosen the captive 8-32 Phillips head screw at the left end of the module. Slide the audio amplifier module to the left until the alignment pins clear the nylon bushings in the center chassis partition and lift directly upward. Replacement is the reverse of removal.

5-32. ALIGNMENT.

5.33 With the exception of the agc/squelch, and noise limiter modules, all remaining modules of the receiver are prealigned at the factory. If it is necessary to replace the antenna coupler, tunable filter, oscillator or mixer multiplier modules perform the tuning and checkout procedures of paragraph 3-11 or 3-12 as applicable. After replacement of any other module complete the receiver performance test procedure, table 5-9. If the synthesizer is being used in place of the crystal oscillator, or if the frequency has drifted off slightly after long-term usage, refer to the following section for minor re-adjustment.

5-33A. OSCILLATOR SYNTHESIZER. The only adjustment which may be required is the reference oscillator. This module is a self-contained and sealed unit located below the phase comparator board. A frequency trimming capacitor is accessible through the sealed case by removal of a sealed screw cover. This is located directly behind the snap-out hole plug which is on the left front of the synthesizer. Turn power off with the front panel switch. Remove receiver top cover. Disconnect oscillator synthesizer output at P2 from mixer/multiplier module, connect frequency counter to P2 connector utilizing subminiature rf connector adaptor P/N 50-075-6801. Then open the front panel door of the parent equipment. Snap out the hole plug on the left front of the DIGI CHANNEL. Use a standard screw, launcher type (split blade) screwdriver to remove the screw cover. With the unit near room ambient temperature, reapply power and wait at least 10 minutes before adjusting. Using a small tuning tool or small blade screwdriver, adjust the trimming capacitor for the dialed frequency. The adjustment is necessary when the frequency is not within ±0.0005% of the desired frequency. NOTE: Refer to Table 3-2A (page 3-6) for actual frequency vs. dialed frequency. Notice that a small portion of a turn may shift the frequency sufficiently. When adjustment is complete, remove power and reinstall the screw cover and then the hole plug.

Table 5-9. Performance Test of VHF and UHF Receivers

STEP	TEST EQUIPMENT	POINT OF TEST	OPERATION OF EQUIPMENT	PERFORMANCE STANDARD
1	Turn signal generator on.		Turn receiver on.	
2	Set signal generator to same frequency receiver is set. Allow 30 minutes warmup for signal generator to stabilize.			
3	Connect voltmeter set on 10 VDC scale, between AGC and GROUND test points on receiver.	AGC test point.	Remove coaxial jumper between RECEIVER INPUT and ANTENNA connectors on front panel of receiver.	
4	Connect signal generator to RECEIVER INPUT connector.		Place receiver SQUELCH switch to OFF.	
5	Set signal generator to −97.5 dbm (3.0 μv) ± 0.5 dbm, 30% modulation at 1 khz ± 10%. Carefully adjust signal generator frequency, using both COARSE and FINE frequency controls, for maximum agc voltage. NOTE If signal generator has not stabilized sufficiently, and continues to drift in frequency this step should be repeated at intervals to assure that signal generator is on frequency.			Maximum agc voltage.
6	Set voltmeter on 300 millivolt ac scale and connect between IF and ground test points.	IF test point	If adjustment is necessary; adjust AGC ADJUST potentiometer on agc/squelch module. (AGC ADJUST is accessible through top cover of receiver.)	125 ± 5 millivolts ac (This setting may be changed later.)

Table 5-9. Performance Test of VHF and UHF Receivers (Cont.)

STEP	TEST EQUIPMENT	POINT OF TEST	OPERATION OF EQUIPMENT	PERFORMANCE STANDARD
7	Set voltmeter on 10 vdc scale and connect to AGC test point. Reduce signal generator power to -120 dbm (0.224 μv) ±1 dbm.	AGC test point		Agc voltage drops to its quiescent value of +2.9 vdc ±0.3 vdc.
7a			If voltage does not drop adjust AGC ADJUST through top cover until AGC voltage just drops to 2.9 ±0.3 volt.	
8	Set signal generator to -102 dbm (1.78 μv) ±1 dbm	AGC test point		AGC voltage is 5.0 volts or greater.
9	Set signal generator to -97.5 dbm (3.0 μv) ±1 dbm 30 percent ±1% modulation at 1 khz ±10%.			The 125 ±5 mv reading obtained in step 6 may now read between 120 and 180 mv.
			NOTE The following step 10 is to be performed only when early configuration AGC/Squelch module, P/N 8004239G1, is installed. After step 10 only is completed, continue at step 11. When later configuration AGC/Squelch module is installed, step 9 should be followed by step 10A.	
10	Set voltmeter on 3 vac scale and connect between MAIN AF and GROUND test points.	MAIN AF test point	Adjust receiver AUDIO MAIN ADJ potentiometer maximum clockwise. If voltage is too high, there is a fault in receiver. If voltage is too low, adjust AF PREAMPL on agc module until 1.5 vac level is obtained. (AF PREAMPL is accessible through top cover of receiver).	Voltmeter indicates 1.5 vac to 2.5 vac.

Table 5-9. Performance Test of VHF and UHF Receivers (Cont.)

STEP	TEST EQUIPMENT	POINT OF TEST	OPERATION OF EQUIPMENT	PERFORMANCE STANDARD
			NOTE Continue performance test at step 11.	
10A	Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND test point.	MAIN AF test point	Remove Receiver top cover. Adjust Compression Level (R41) on AGC/Squelch module maximum clockwise.	
			Adjust AUDIO MAIN ADJ control maximum clockwise.	2.00 vac ±25 millivolts.
			If Performance Standard is not met, adjust AF Preamp Adj (R32) on AGC/Squelch module for 2.00 vac ±25 millivolts.	
10B	Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND test point.	MAIN AF test point	Adjust AUDIO MAIN ADJ level control on front panel of receiver.	1.6 vac ±25 millivolts.
10C	Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND test point.	MAIN AF test point	Readjust AF Preamp Adj (R32)	2.00 vac ±25 millivolts.
10D	Set voltmeter to 3 vac scale and connect between MAIN AF test point and GROUND test point.	MAIN AF test point	Adjust Compression Level control (R41) on AGC module.	1.95 vac ±10 millivolts.
10E	Increase signal generator percent modulation from 30% to 90%.	MAIN AF test point		Test voltage shall remain within 1.75 to 2.45 volts.

Table 5-9. Performance Test of VHF and UHF Receivers (Cont.)

STEP	TEST EQUIPMENT	POINT OF TEST	OPERATION OF EQUIPMENT	PERFORMANCE STANDARD
11	Observe that signal generator is still set at -97.5 dbm (3.0 μv) ±0.5 dbm 30 percent ±1% modulated at 1 khz ±10%.		Adjust receiver AUDIO MAIN ADJ potentiometer for 1.0 vac.	Voltmeter indicates 1.0 vac.
12	Set voltmeter to 1 vac scale.			
13	Switch signal generator to CW mode (-97.5 dbm) (3.0 μv) ±0.5 dbm.			Voltmeter drop to less than .316 vac or less than -10 dbm
14	Set signal generator at -97.5 dbm (3.0 μv) ±0.5 dbm 30 percent ±1% modulated at 1 khz ±10%.			
15	Set voltmeter to 3 vac scale.		Adjust receiver AUDIO MAIN ADJ potentiometer for 1.0 vac.	Voltmeter indicates 1.0 ±0.5 vac.
16	Connect earphones to AUDIO OUTPUT jack.	PHONE jack	Adjust AUDIO PHONE ADJ potentiometer for comfortable listening level.	
17	While maintaining modulation level at 30 percent, slowly adjust power level of signal generator from -97.5 dbm (3.0 μv) ±0.5 dbm to +13 dbm (999 mv) ± 10 mv.			Observe highest and lowest excursion of voltage on DB scale of meter. Highest and lowest reading should not differ more than 3 db (in terms of voltage V min/V max should be 0.7 or greater).
	While changing power level of signal generator observe indications listed in Performance Standard Column.			Tone in earphones should not exhibit excessive distortion to the ear; i.e. 10% or less as measured on a distortion analyzer.

Table 5-9. Performance Test of VHF and UHF Receiver (Cont.)

STEP	TEST EQUIPMENT	POINT OF TEST	OPERATION OF EQUIPMENT	PERFORMANCE STANDARD
18	Set signal generator to -97.5 dbm (3.0 μv) ±0.5 dbm modulated 30 percent ±10% at 1 kHz ±10%.		Set receiver AUDIO SQUELCH ADJ potentiometer maximum counterclockwise.	
			Set receiver SQUELCH switch to ON.	Audio should remain fully audible and unchanged in earphones (receiver should not be squelched).
19			Set receiver AUDIO SQUELCH ADJ potentiometer maximum clockwise.	Receiver squelched (quieted).
20	Raise signal generator power level to -73 dbm (50.1 μv) ±0.5 dbm.			Receiver remains squelched.
21	Set signal generator at desired level (the level must be between -97.5 dbm and -73 dbm).	Squelch Test Point	Slowly turn the audio squelch adj potentiometer CCW. Place voltmeter range selector switch to 30V scale. Place voltmeter DC probe in receiver squelch jack.	Voltmeter should suddenly increase either to approximately 15 Vdc (squelch voltage) for early configuration AGC module or to approximately 8 Vdc for later configuration AGC module.
22	Set signal generator to off, and disconnect from receiver.		Replace coaxial jumper between ANTENNA and RECEIVER INPUT connector on front panel of receiver.	

CHAPTER 6

CIRCUIT DIAGRAMS

6-1. INTRODUCTION. This chapter contains block diagrams, schematic diagrams, and a wiring list necessary to support the theory and maintenance of the VHF and UHF receivers.

Table 6-1. Receiver Wire List

WIRE NUMBER	FROM TERMINAL CONNECTOR	PIN	CONN LUG	TO TERMINAL CONNECTOR	PIN	CONN LUG	TYPE	GAUGE	COLOR	EST. LENGTH INCHES	EIGHTH	NOTES	REMARKS
1	J15	16	2	E4		4	E	22	0	9	0		
2	J15	14	2	J3	2	DF	E	22	7	11	4		
3	J15	13	2	J3	3	DF	E	22	2	11	6		
4	J15	12	2	J4	13	DF	E	22	4	13	4		
5	J15	11	2	J4	8	DF	E	22	9	13	6		
6	J15	10	2	J9	8	DF	Y	22	5	15	4	1	Shielded
7	J15	9	2	J6	5	DF	E	22	6	15	4		
8	J15	8	2	J7	7	DF	E	22	95	13	0		
9	J15	6	2	J6	6	DF	E	22	1	16	2		
10	J15	4	2	J7	11	DF	E	22	96	13	6		
11	J15	3	2	J8	5	DF	E	22	93	16	0		
12	J15	2	2	J4	7	DF	E	22	90	16	0		
13	J15	1	2	J5	8	DF	E	22	8	18	4		
14	J14	T	4	J5	13	DF	E	22	96	16	4		
15	J14	R	4	J5	12	DF	E	22	95	16	4		
16	S1	1	4	J4	15	DF	E	22	91	5	0		
17	S1	2	4	R1	1	2	E	22	9	4	0		
18	S1	3	4	J4	9	DF	E	22	3	15	0		
19	R1	2	4	J4	10	DF	E	22	7	14	4		
20	R1	3	2	J4	11	DF	E	22	8	14	4		
21	R3	1	2	R2	1	2	E	22	1	4	0		
22	R3	1	2	J4	5	DF	E	22	1	15	4		
23	R3	3	2	R2	3	2	E	20	0	4	0		
24	R3	3	2	E4		4	E	20	0	10	6		
25	R3	2	2	J5	7	DF	E	22	7	17	0		
26	R2	2	2	J5	5	DF	E	22	90	16	6		
27	J3	1	DF	E3		4	E	20	0	4	2		
28	J3	4	DF	J6	3	DF	E	22	2	9	0		
29	J3	6	DF	J7	3	DF	E	22	2	6	4		
30	J3	8	DF	J8	3	DF	E	20	2	8	4		
31	J3	9	DF	J9	3	DF	E	20	2	9	0		
32	J3	10	DF	J4	3	DF	E	20	2	8	4		
33	J3	11	DF	J5	3	DF	E	20	2	10	2		
34	J3	12	DF	J6	2	DF	E	22	7	8	6		
35	J4	1	DF	E3		4	E	20	0	4	0		
37	J4	6	DF	J5	15	DF	E	22	6	8	6		
38	J4	14	DF	E6		2	E	22	5	6	0		

Table 6-1. Receiver Wire List (Cont.)

WIRE NUMBER	FROM TERMINAL CONNECTOR	PIN	CONN LUG	TO TERMINAL CONNECTOR	PIN	CONN LUG	TYPE	GAUGE	COLOR	EST. LENGTH INCHES	EST. LENGTH EIGHTH	NOTES	REMARKS
39	J5	1	DF	E2		4	E	20	0	4	2		
40	J5	9	DF	C2	1	2S	E	22	4	11	2	2	
41	J5	11	DF	C3	1	2S	E	22	3	11	2	2	
42	J5	10	DF	C4	1	2S	E	22	9	11	2	2	
43	J7	1	DF	E7		4	E	20	0	7	4		
44	J7	5	DF	E6		2	E	22	5	4	0		
45	J6	1	DF	E7		4	E	20	0	3	0		
46	J8	1	DF	E7		4	E	20	0	7	4		
47	J9	9	DF	E6		2	E	22	5	10	0		
48	J9	1	DF	E5		4	E	20	0	5	0		
49	J9	5	DF	C5		2S	Y	22	6	10	0	3 & 2	Shielded
50	J9	7	DF	J4	12	DF	E	22	95	7	6		
53	C1	1	2S	E6		2	E	22	5	14	0	2	
54	C8	1	2S	XF3	1	4	E	22	6	23	6	2	
55	XF3	2	4	S2	3	4	E	22	7	9	4		
56	S2	7	4	J3	7	DF	E	22	6	18	0		
60	J3	5	DF	J6	4	DF	E	22	92	7	0		
61	C6	1	2S	XF1	1	4	R	20	8	22	4		Twisted Pair
62	C7	1	2S	XF2	1	4	R	20	98				
63	XF1	2	4	S2	1	4	R	20	1	11	0		Twisted Pair
64	XF2	2	4	S2	2	4	R	20	91				
65	S2	5	4	XDS1	1	4	R	20	8	9	2		Twisted Pair
66	S2	6	4	XDS1	2	4	R	20	98				
67	S2	5	4	J3	14	DF	R	20	8	8	4		Twisted Pair
68	S2	6	4	J3	15	DF	R	20	98				

NOTES – CODE IDENTIFICATION

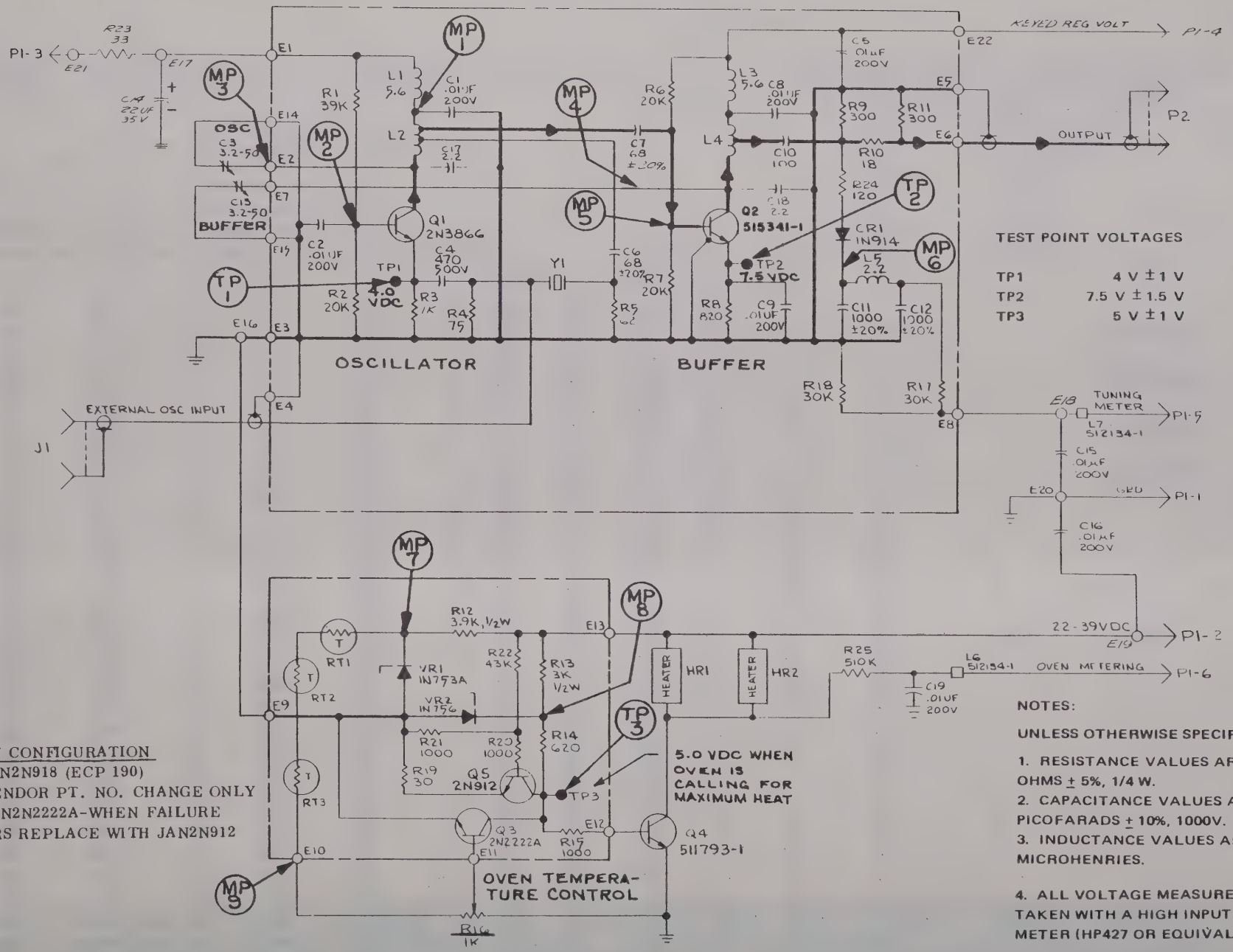
"WIRE NUMBER" COLUMN: NUMBERS 26, 51, 52, 57, 58, and 59 DELETED.

"CONN LUG" COLUMN:
- DF 502056-402 CONTACT, FEMALE
- 2 2/8" STRIP LENGTH
- 4 4/8" STRIP LENGTH

"TYPE" COLUMN:
- E 4590 WIRE
- Y 4596 WIRE, SHIELDED AND JACKETED
- R 517875 WIRE, TWISTED PAIR

"COLOR" COLUMN:
- 0 BLACK
- 1 BROWN
- 2 RED
- 3 ORANGE
- 4 YELLOW
- 5 GREEN
- 6 BLUE
- 7 VIOLET
- 8 GRAY
- 9 WHITE
- 10 BLACK
- 11 ETC. BROWN

"NOTES" COLUMN:
- 1 SOLDER SHIELDS OF WIRE 6 AT E5
- 2 S – DENOTES SLEEVING, INSULATION
- 3 SOLDER SHIELD OF WIRE 49 AT E1 AND E5



EARLY CONFIGURATION
Q2, JAN2N918 (ECP 190)
Q4, VENDOR PT. NO. CHANGE ONLY
Q5, JAN2N2222A-WHEN FAILURE OCCURS REPLACE WITH JAN2N912

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ± 10%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

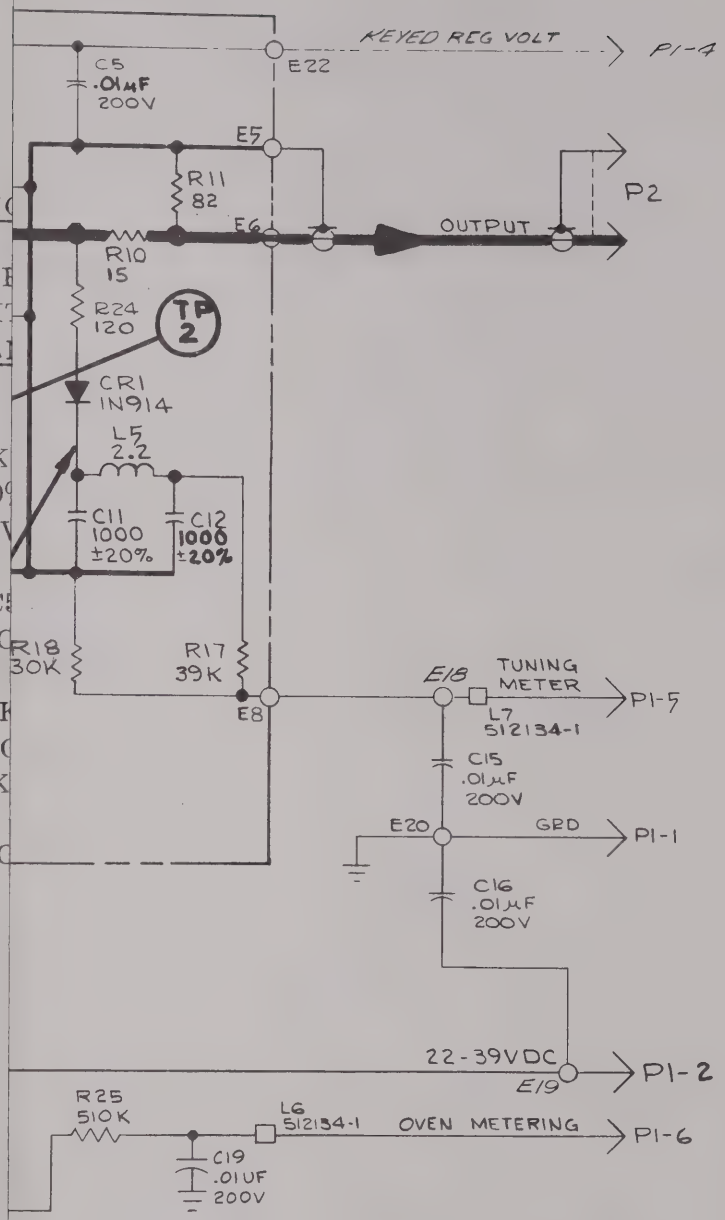
Figure 6-1. Crystal Controlled Oscillator A1; Schematic Diagram (G1)

EARLY CONFIGURATI
Q4, VENDOR PT. NO.
Q5, JAN2N2222A - IF
OCCURS REPLACE WI
CONFIGURATION CHA

R10 FROM 5.6 TO 9.1
R17 FROM 30K TO 24K
C7 FROM ±20% TO ±10
C20 FROM ±10%, 1000V

R9 DELETED FROM C
R10 FROM 9.1 TO 15 C
R11 FROM 910 TO 300
R14 FROM 620 TO 1.2K
R15 FROM 1K TO 100 C
R17 FROM 24K TO 39K

R11 FROM 300 TO 82 C



	UNKEYED	KEYED
TP1	5.0 VDC	5.0 VDC
TP2	0 VDC	7.0 VDC
TP3	3.8 VDC	4.0 VDC

d Oscillator A1, Schematic Diagram* (G2)

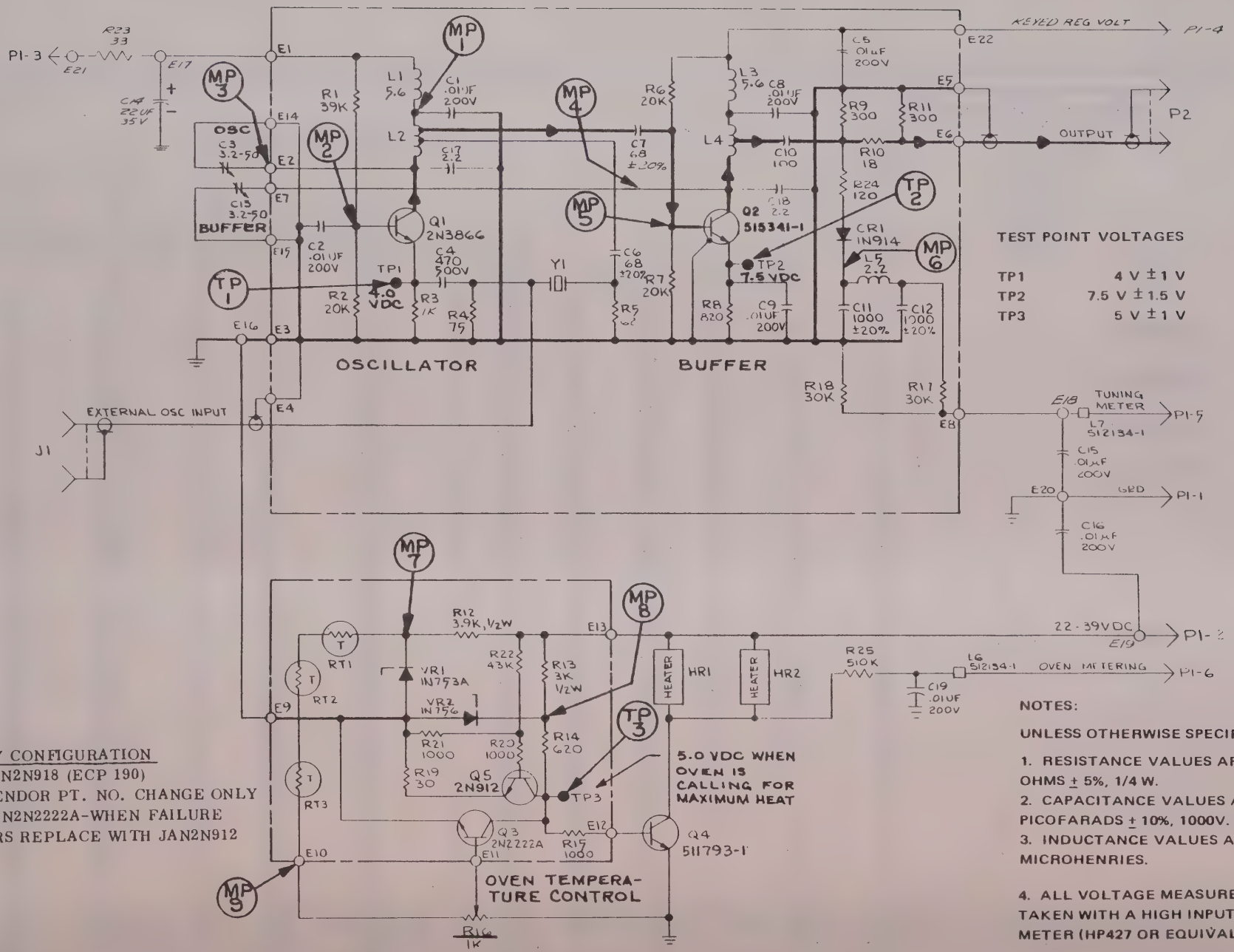


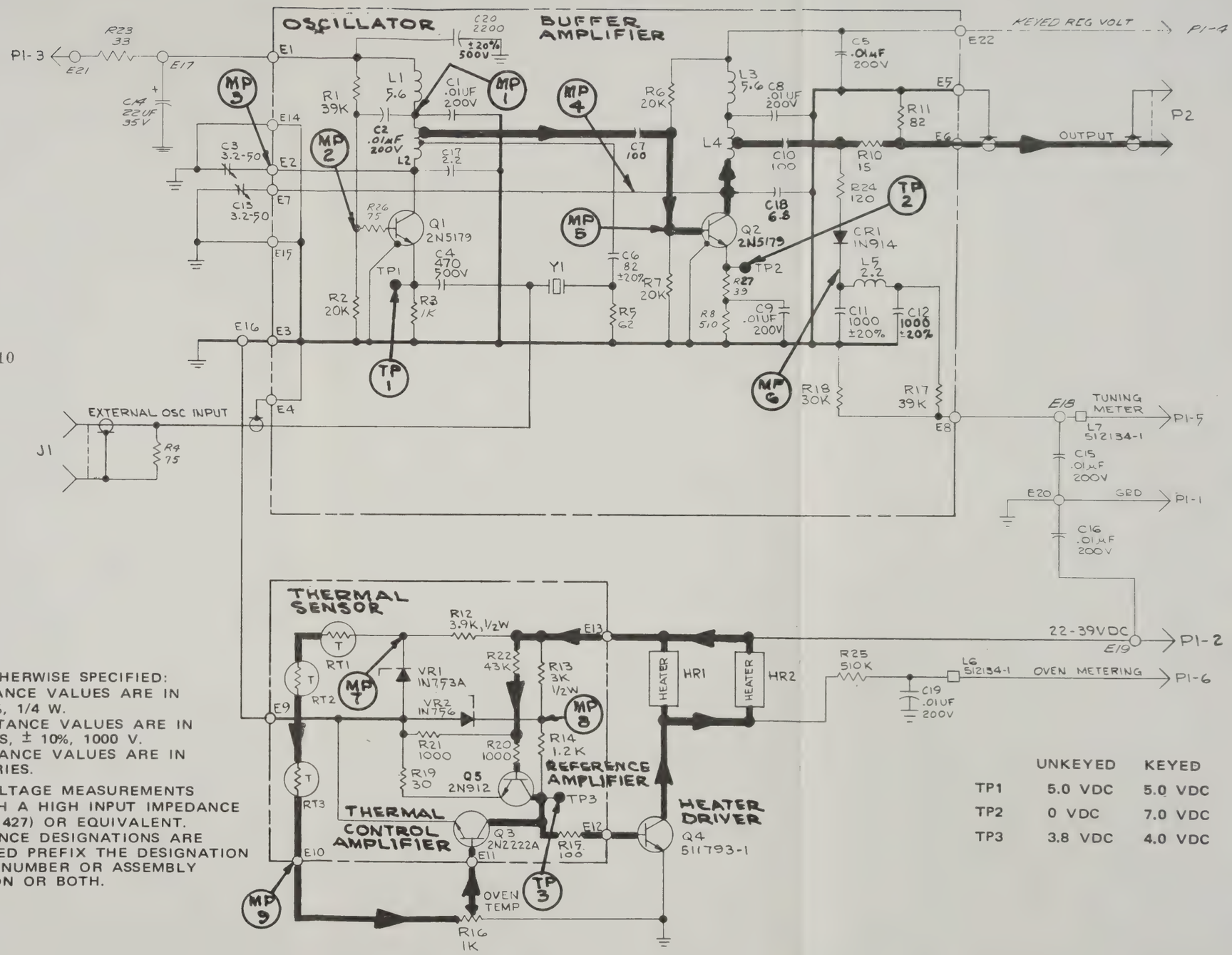
Figure 6-1. Crystal Controlled Oscillator A1, Schematic Diagram (G1)

EARLY CONFIGURATION
Q4, VENDOR PT. NO. CHANGE ONLY
Q5, JAN2N2222A - IF FAILURE OCCURS REPLACE WITH JAN2N912.
CONFIGURATION CHANGES

R10 FROM 5.6 TO 9.1 OHMS
R17 FROM 30K TO 24K
C7 FROM ±20% TO ±10%
C20 FROM ±10%, 1000V TO ±20%, 500V

R9 DELETED FROM C5 & E5 TO C10 & R10
R10 FROM 9.1 TO 15 OHMS
R11 FROM 910 TO 300 OHMS
R14 FROM 620 TO 1.2K
R15 FROM 1K TO 100 OHMS
R17 FROM 24K TO 39K

R11 FROM 300 TO 82 OHMS



NOTES:

UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS, ± 10%, 1000 V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP 427) OR EQUIVALENT.
5. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

	UNKEYED	KEYED
TP1	5.0 VDC	5.0 VDC
TP2	0 VDC	7.0 VDC
TP3	3.8 VDC	4.0 VDC

Figure 6-2. Crystal Controlled Oscillator A1, Schematic Diagram*(G2)

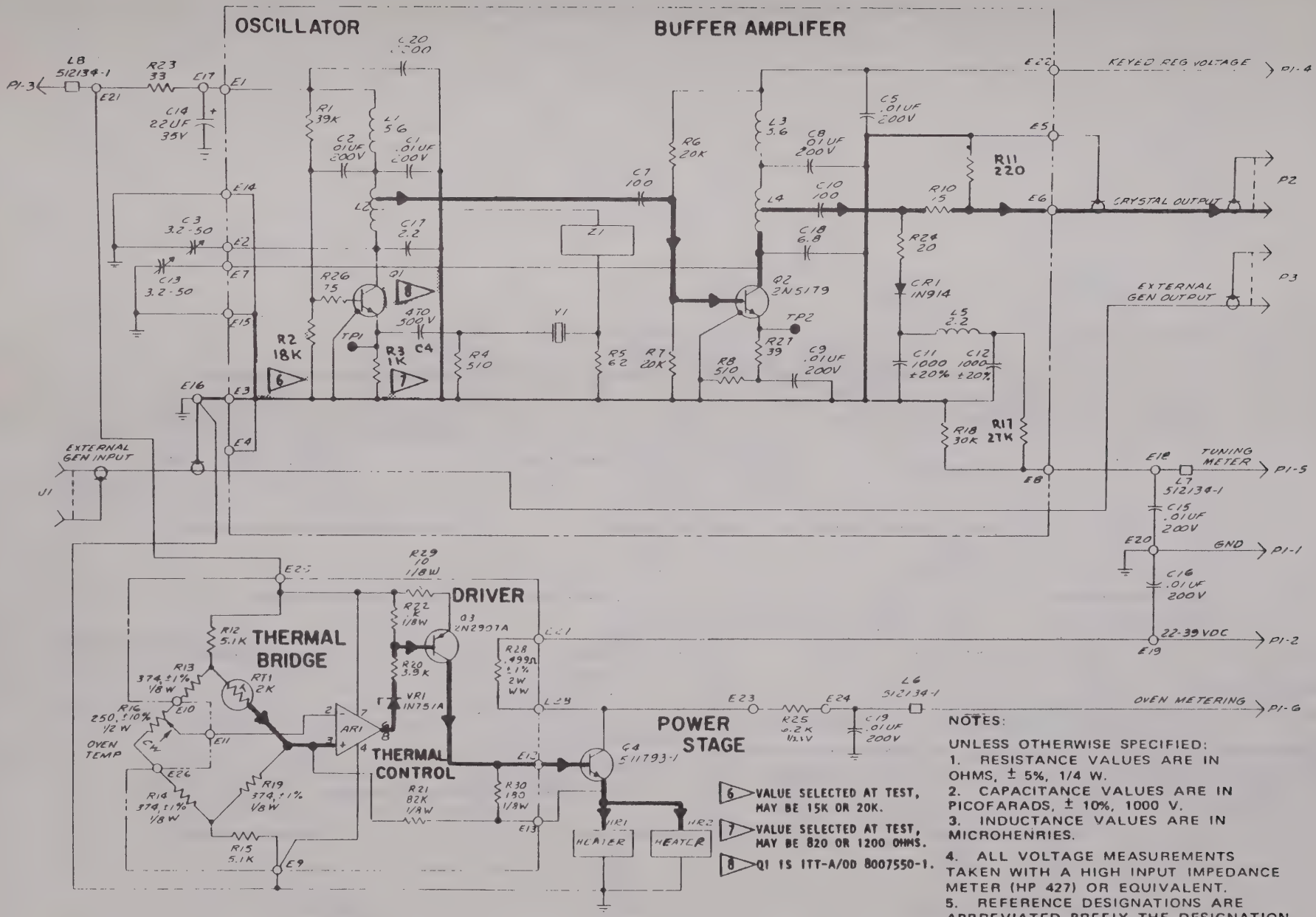

OSCILLATOR
BUFFER AMPLIFER
KEYED REG VOLTAGE
CRYSTAL OUTPUT
EXTERNAL GEN OUTPUT
EXTERNAL GEN INPUT
TUNING METER
GND
22-39 VDC
OVEN METERING
THERMAL BRIDGE
DRIVER
THERMAL CONTROL
POWER STAGE
OVEN TEMP
HEATER
HEATER
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS, ± 10%, 1000 V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP 427) OR EQUIVALENT.
5. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
6 VALUE SELECTED AT TEST, MAY BE 15K OR 20K.
7 VALUE SELECTED AT TEST, MAY BE 820 OR 1200 OHMS.
8 Q1 IS ITT-A/OD 8007550-1.

Figure 6-2A. Crystal Controlled Oscillator A1, Schematic Diagram. (G3)

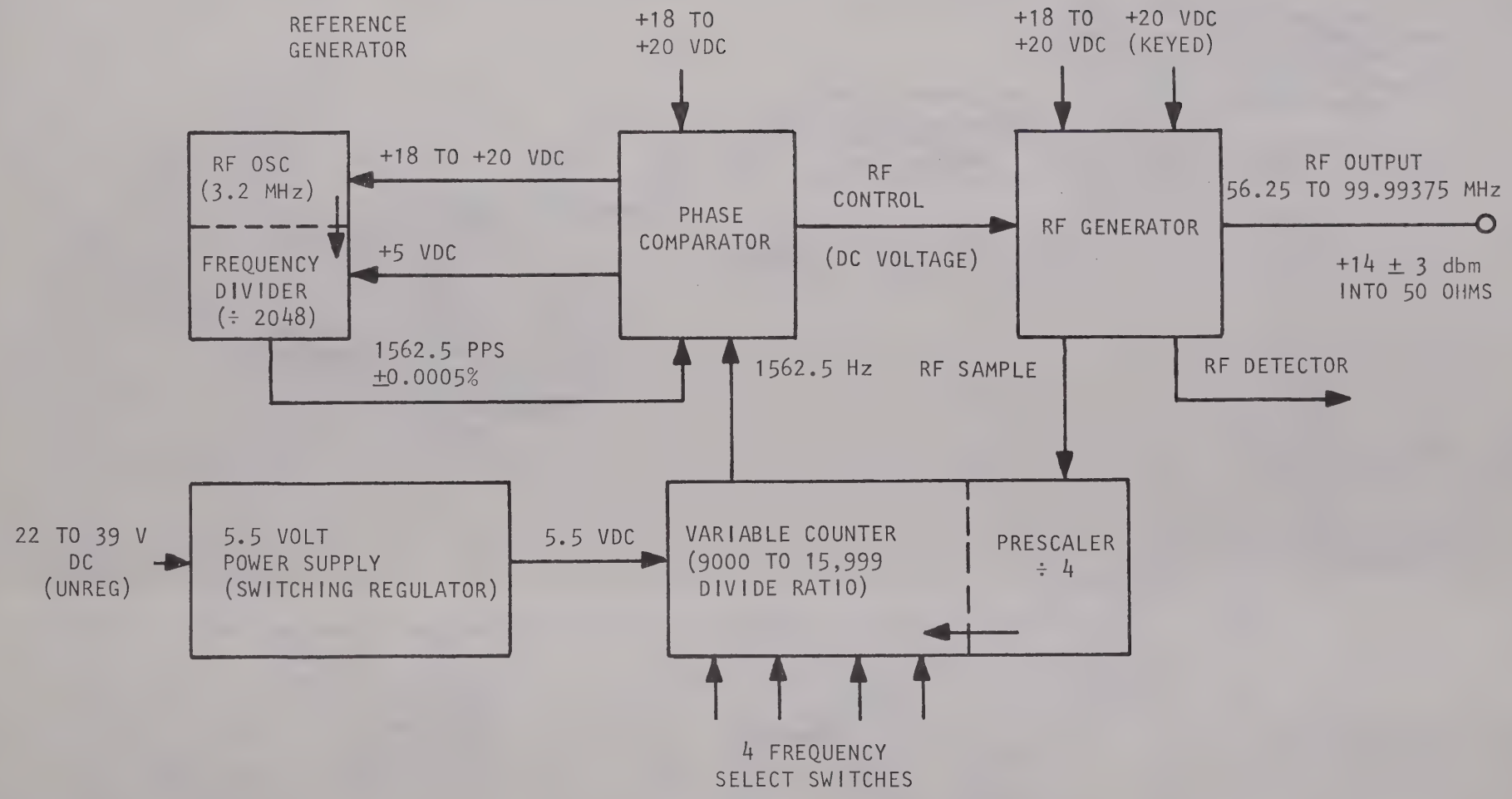
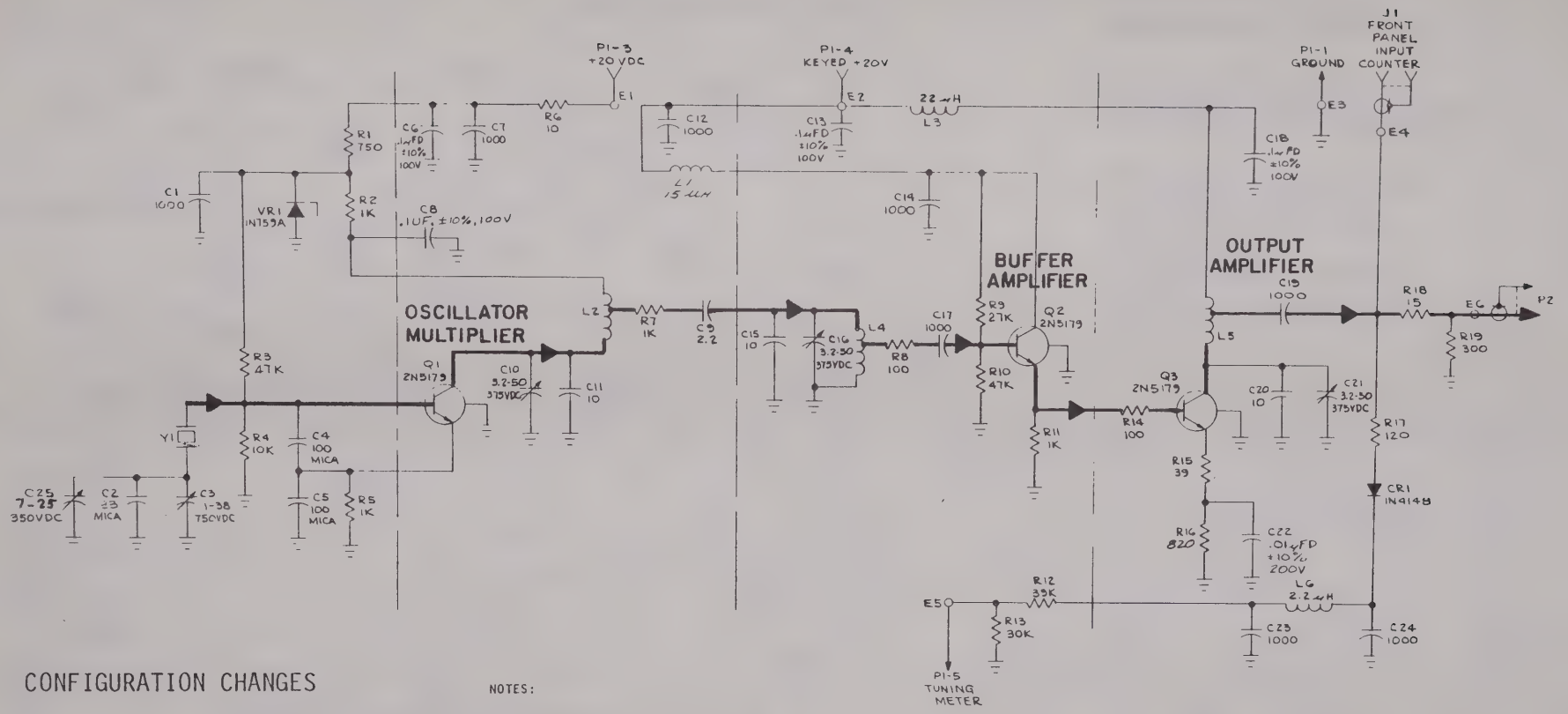


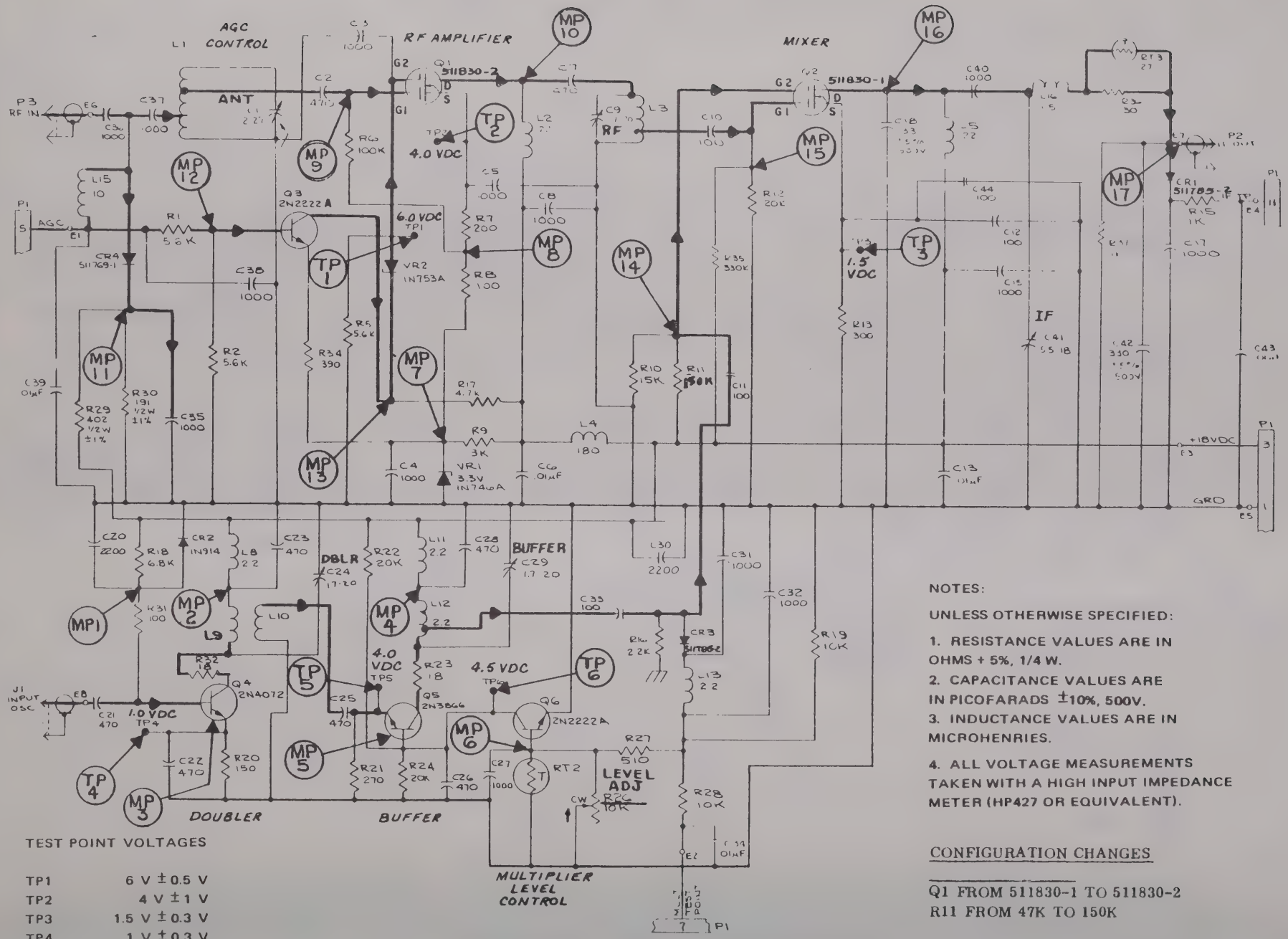
Figure 6-2B. Oscillator-Synthesizer


P1-3 +20 VDC
P1-4 KEYED +20V
P1-1 GROUND
J1 FRONT PANEL INPUT COUNTER
OSCILLATOR MULTIPLIER
BUFFER AMPLIFIER
OUTPUT AMPLIFIER
P1-5 TUNING METER
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS * 5%, 1/4W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ± 10%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).
REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH

CONFIGURATION CHANGES

C25 FROM 5.5-18 TO 7-25 pF

Figure 6-2C. Oscillator-Multiplier A1, Schematic Diagram



TEST POINT VOLTAGES

TP1	6 V ±0.5 V
TP2	4 V ±1 V
TP3	1.5 V ±0.3 V
TP4	1 V ±0.3 V
TP5	4 V ±1 V
TP6	4.5 V ±1 V

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS + 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ±10%, 500V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

CONFIGURATION CHANGES

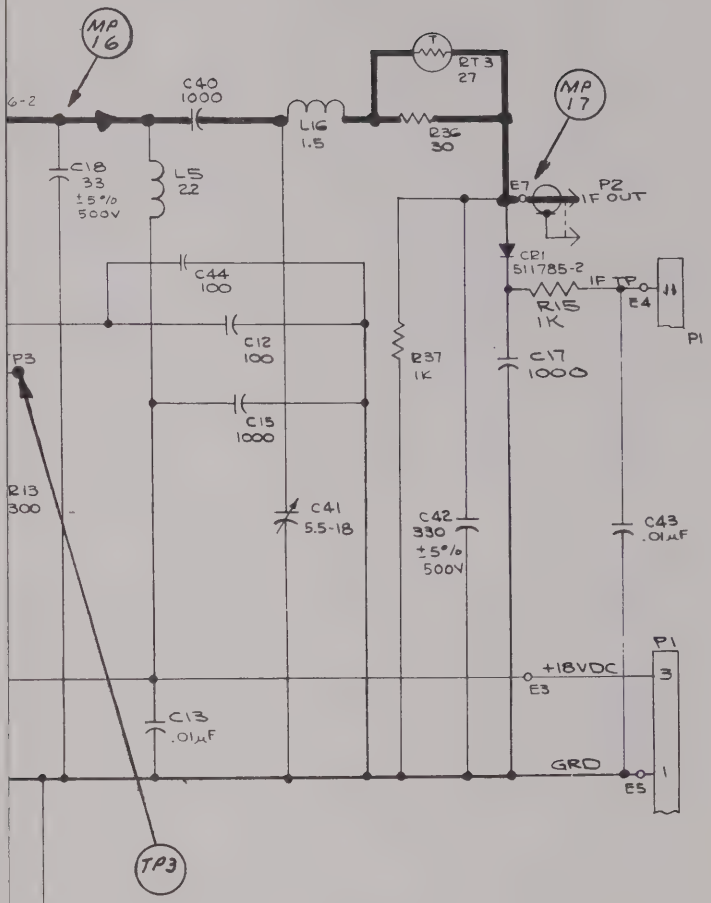
Q1 FROM 511830-1 TO 511830-2
R11 FROM 47K TO 150K

Figure 6-3. Mixer/Multiplier (VHF Receiver) A2, Schematic Diagram (G1)

S

OHENRIES

MS



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. CAPACITANCE CONTAINED WITHIN PC BOARD.
2. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
3. CAPACITANCE VALUES ARE IN MICROMICROFARADS ± 10%, 500 V.
4. INDUCTANCE VALUES ARE IN MICROHENRIES.

5 R38 VALUE MAY BE CHANGED AT TEST TO 10, 20 OR 39 OHMS TO COMPENSATE FOR Q1 GAIN VARIATIONS.

HF Receiver) A2, Schematic Diagram (G2)

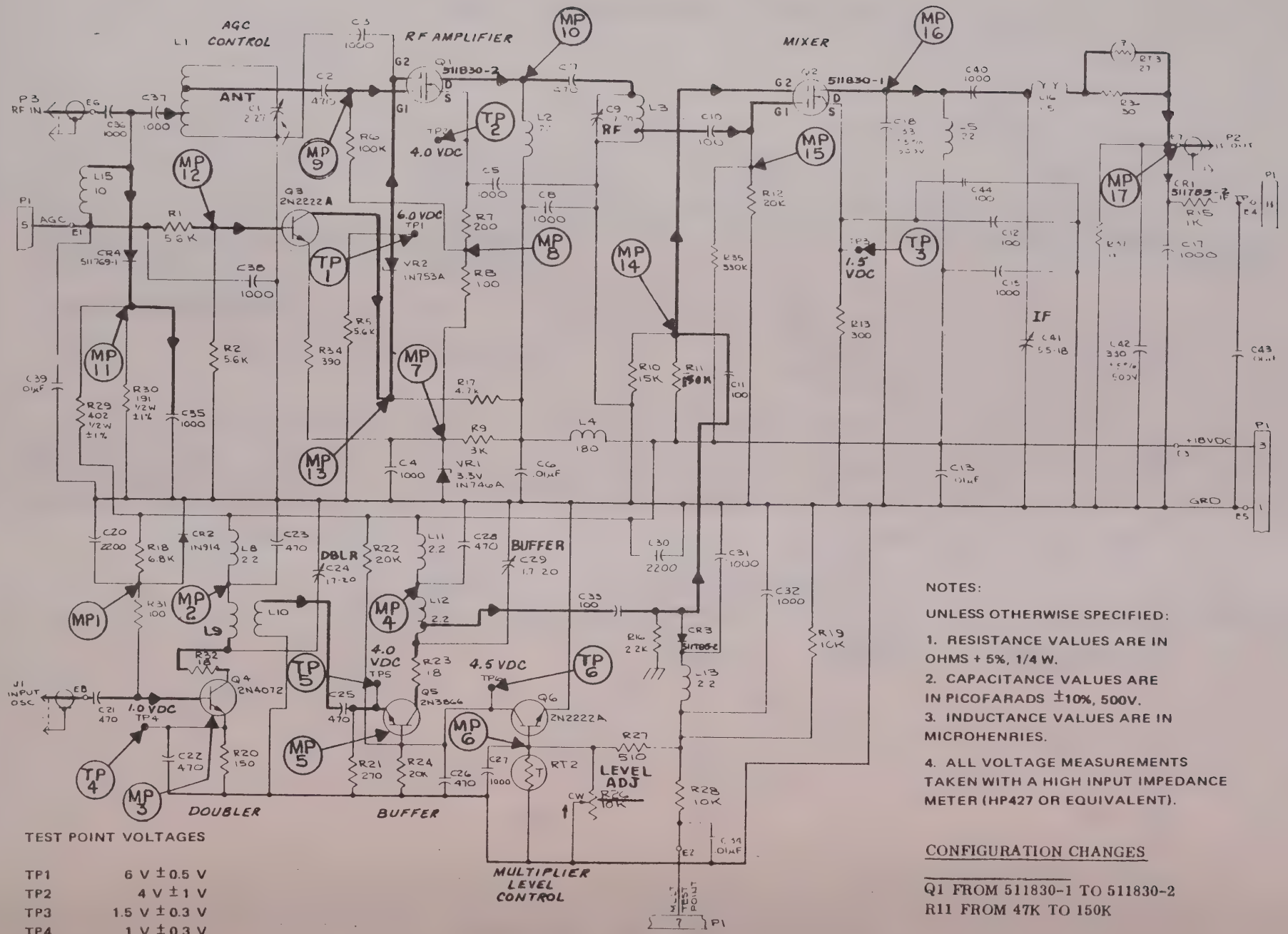


Figure 6-3. Mixer/Multiplier (VHF Receiver) A2, Schematic Diagram (G1)

CONFIGURATION CHANGES

L2 FROM 22 TO 2.2 MICROHENRIES

R34 FROM 390 TO 680 OHMS

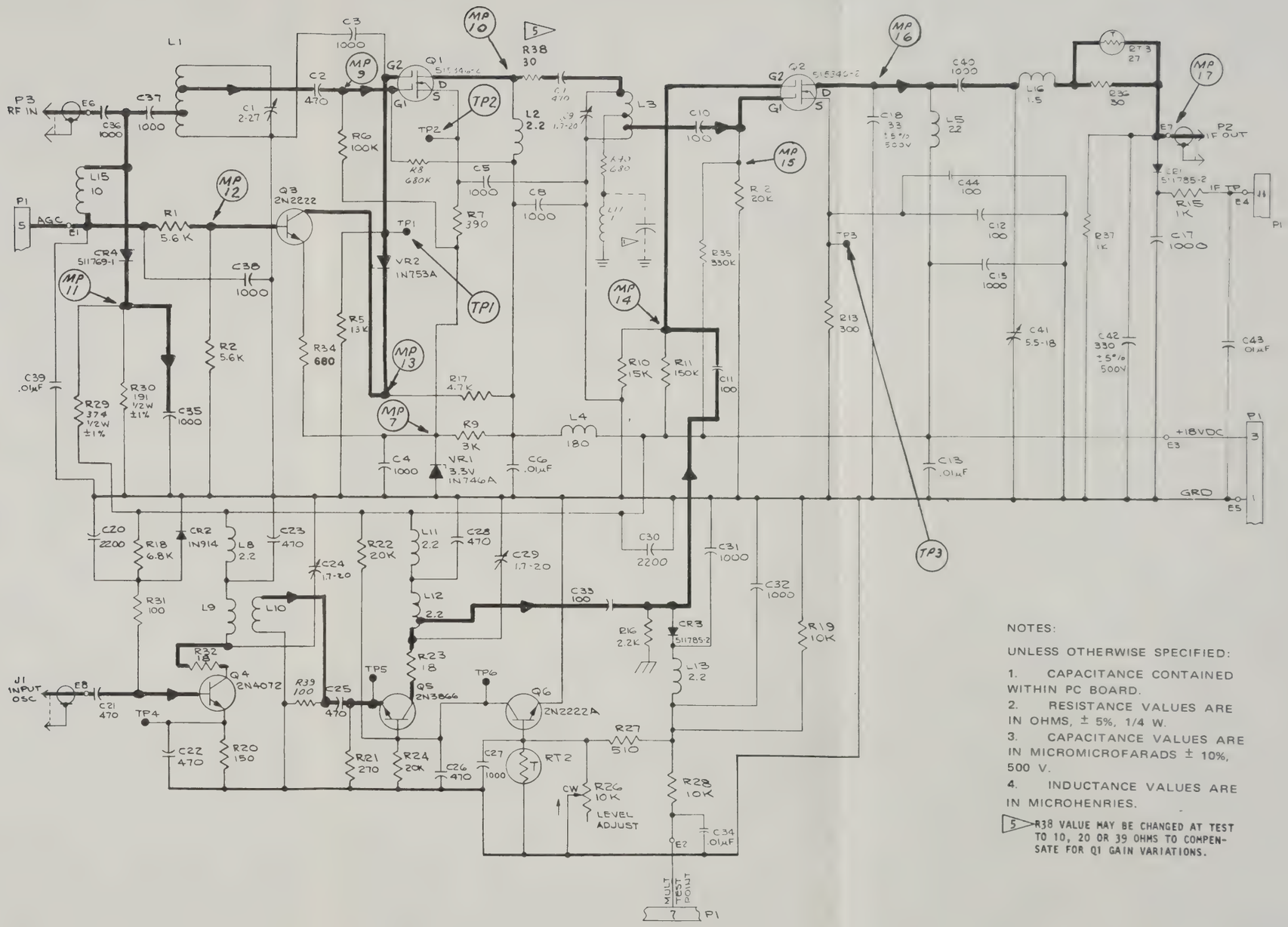
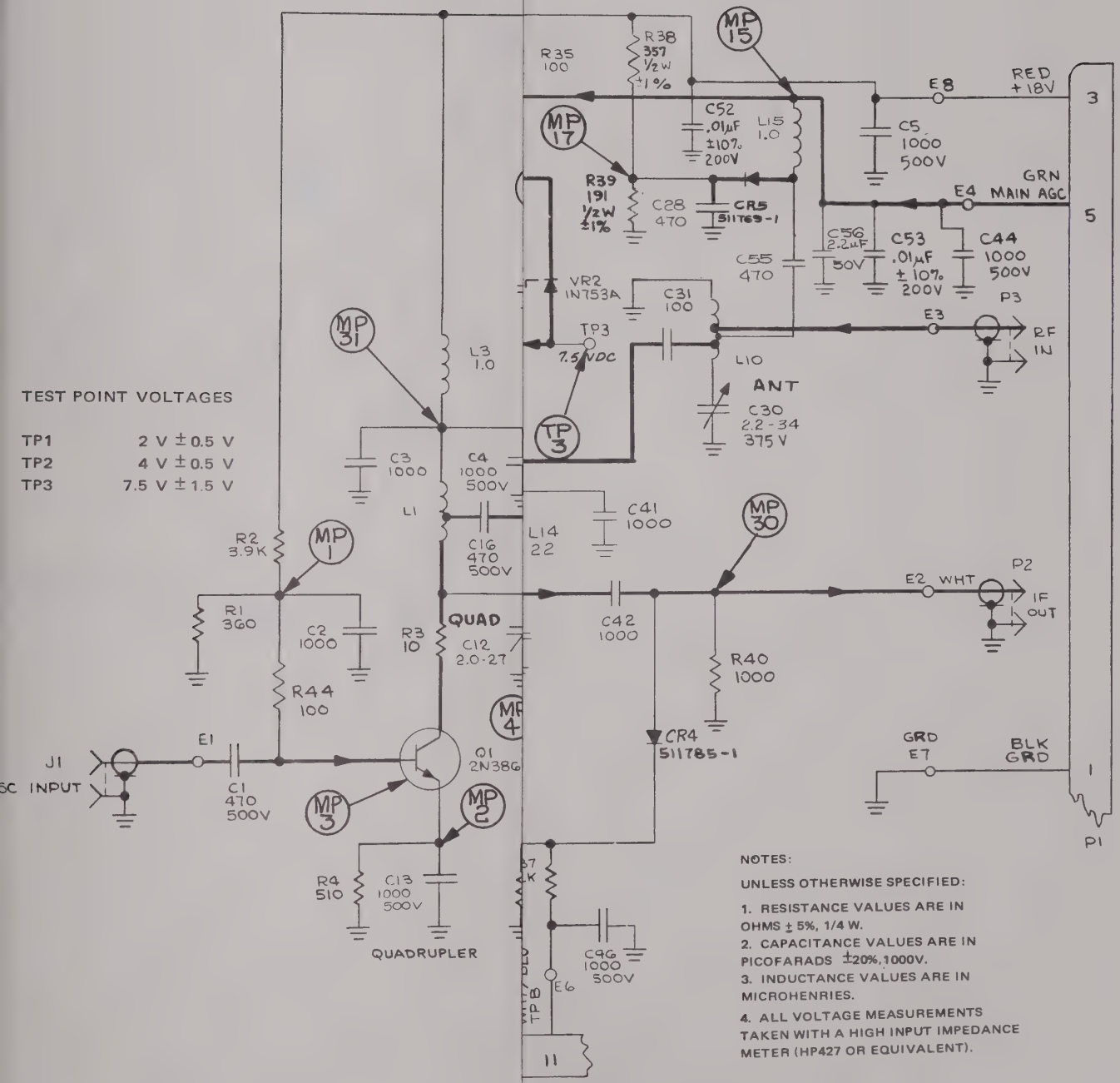


Figure 6-4. Mixer/Multiplier (VHF Receiver) A2, Schematic Diagram (G2).



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ±20%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

(UHF Receiver) A2, Schematic Diagram (G1)

Changed - August, 1980

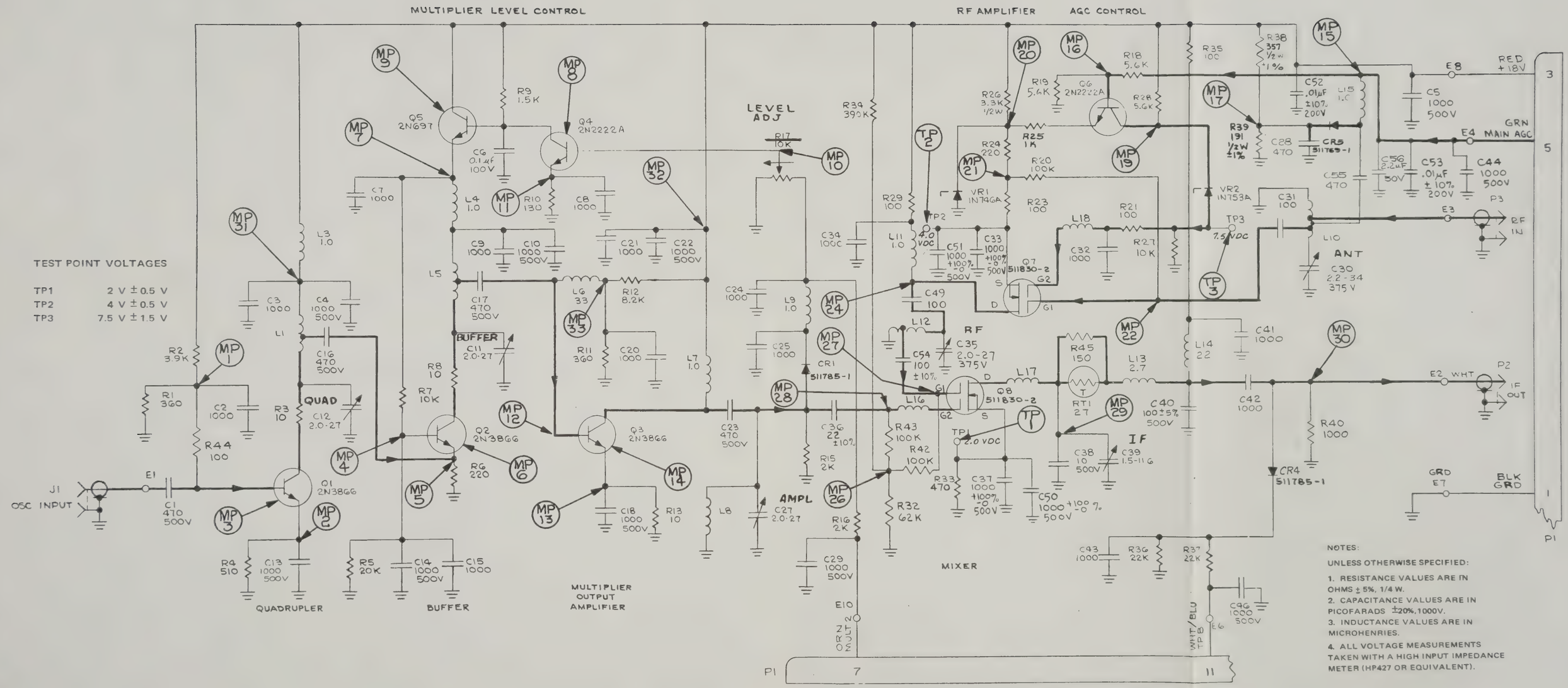
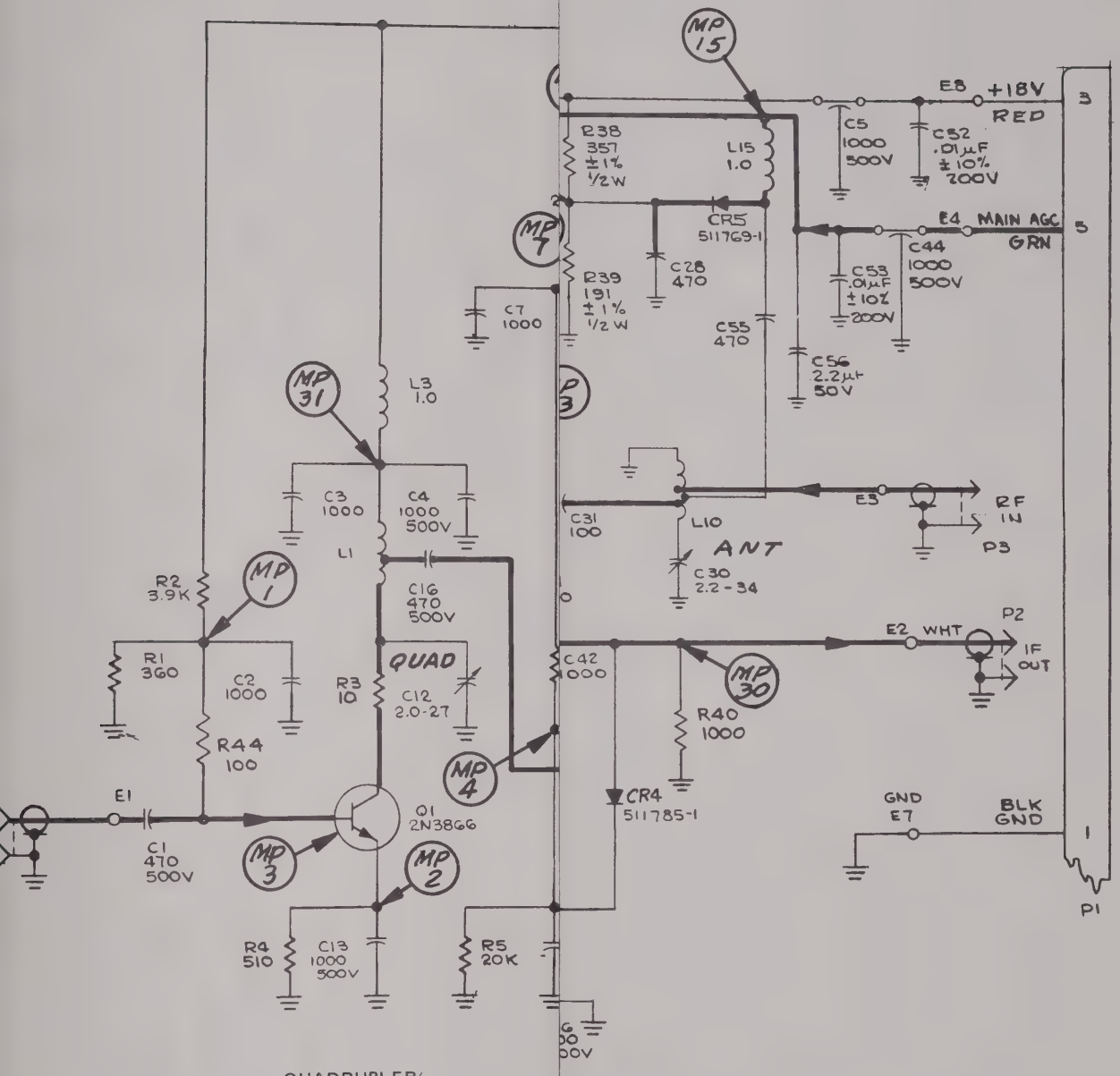


Figure 6-5. Mixer/Multiplier (UHF Receiver) A2, Schematic Diagram (G1)



QUADRUPLER

NOTES:

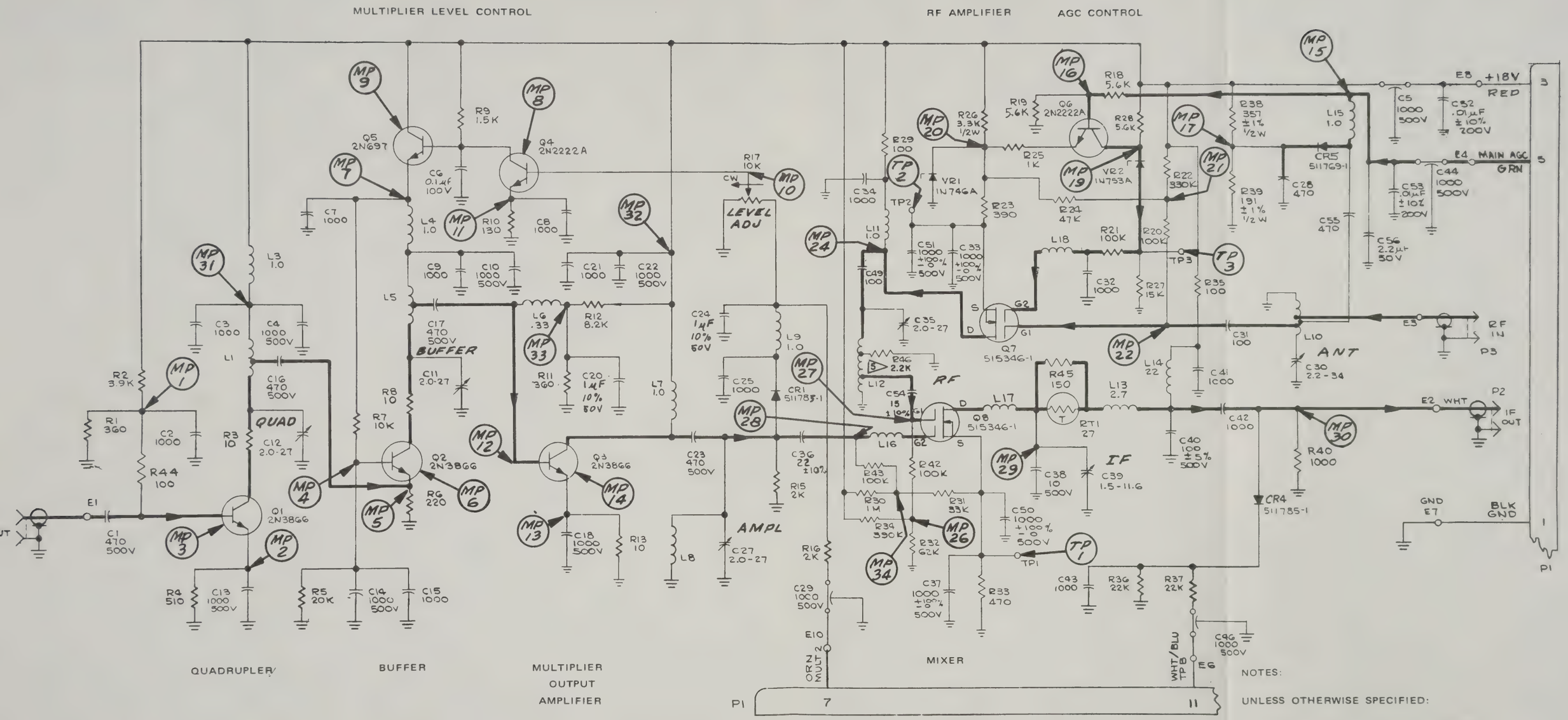
UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS, ± 20%, 1000 V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

5 STANDARD VALUE 2.2K MAY BE CHANGED AT TEST TO 1.5K OR 4.7K TO COMPENSATE TRANSISTOR GAIN VARIATION.

r) A2, Schematic Diagram (G2)

hanged - August, 1980 6–13/(6–14 blank)



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS, ± 20%, 1000 V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

5 STANDARD VALUE 2.2K MAY BE CHANGED AT TEST TO 1.5K OR 4.7K TO COMPENSATE TRANSISTOR GAIN VARIATION.

CONFIGURATION CHANGES

C20 AND C24 FROM 1000 pF TO 1µF, 10%, 50V

R46 FROM 4.7K TO TAILOR POINT 5
C54 FROM 100 TO 15PF, ±10%, 1000V

Figure 6-6. Mixer/Multiplier (UHF Receiver) A2, Schematic Diagram (G2)

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 WATT.
2. ALL CAPACITANCE VALUES ARE IN PICOFARADS ± 20%, 500 VOLTS.
3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES.

4 HEWLETT-PACKARD 5082-8906

5 RCA 2N5109

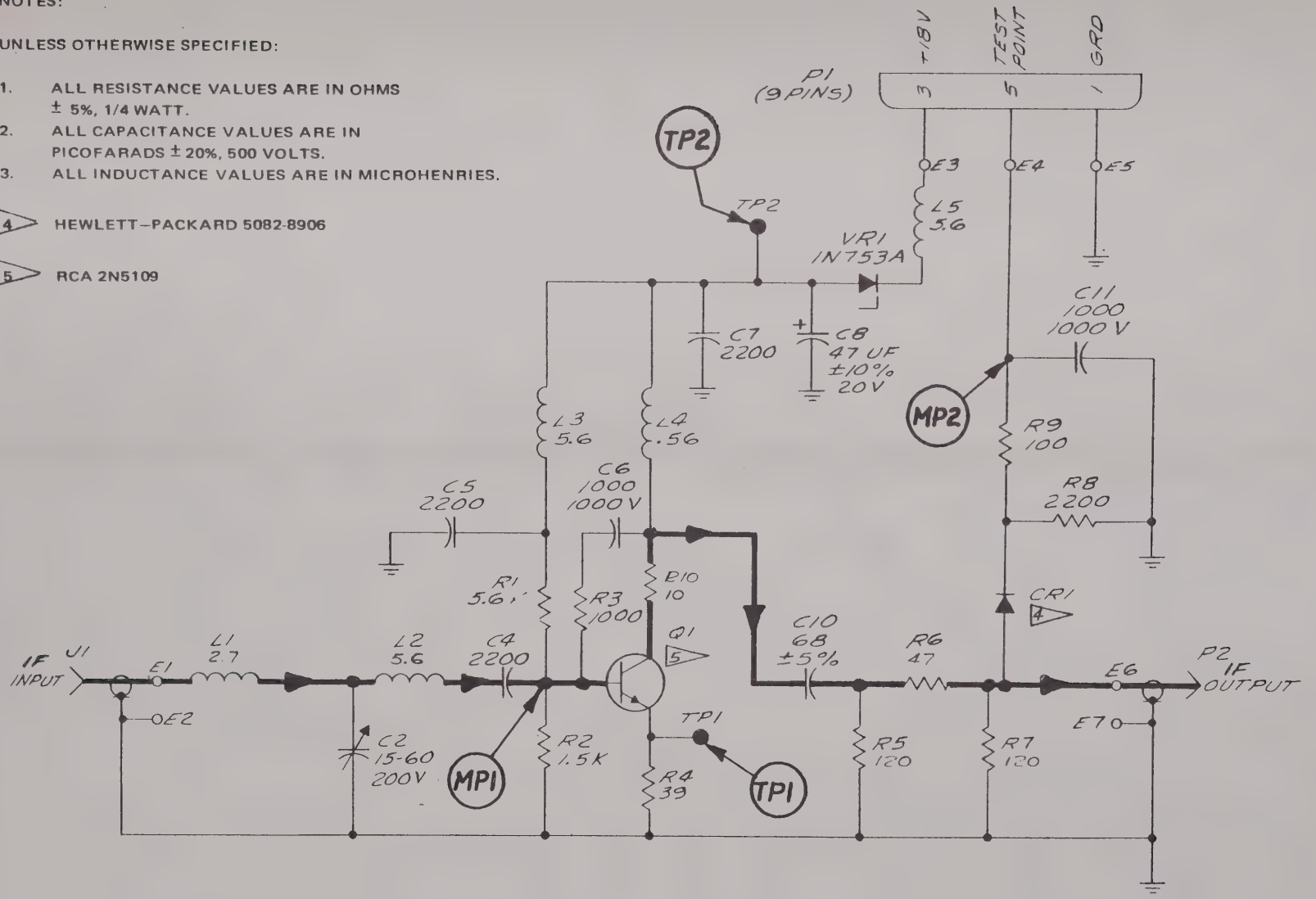
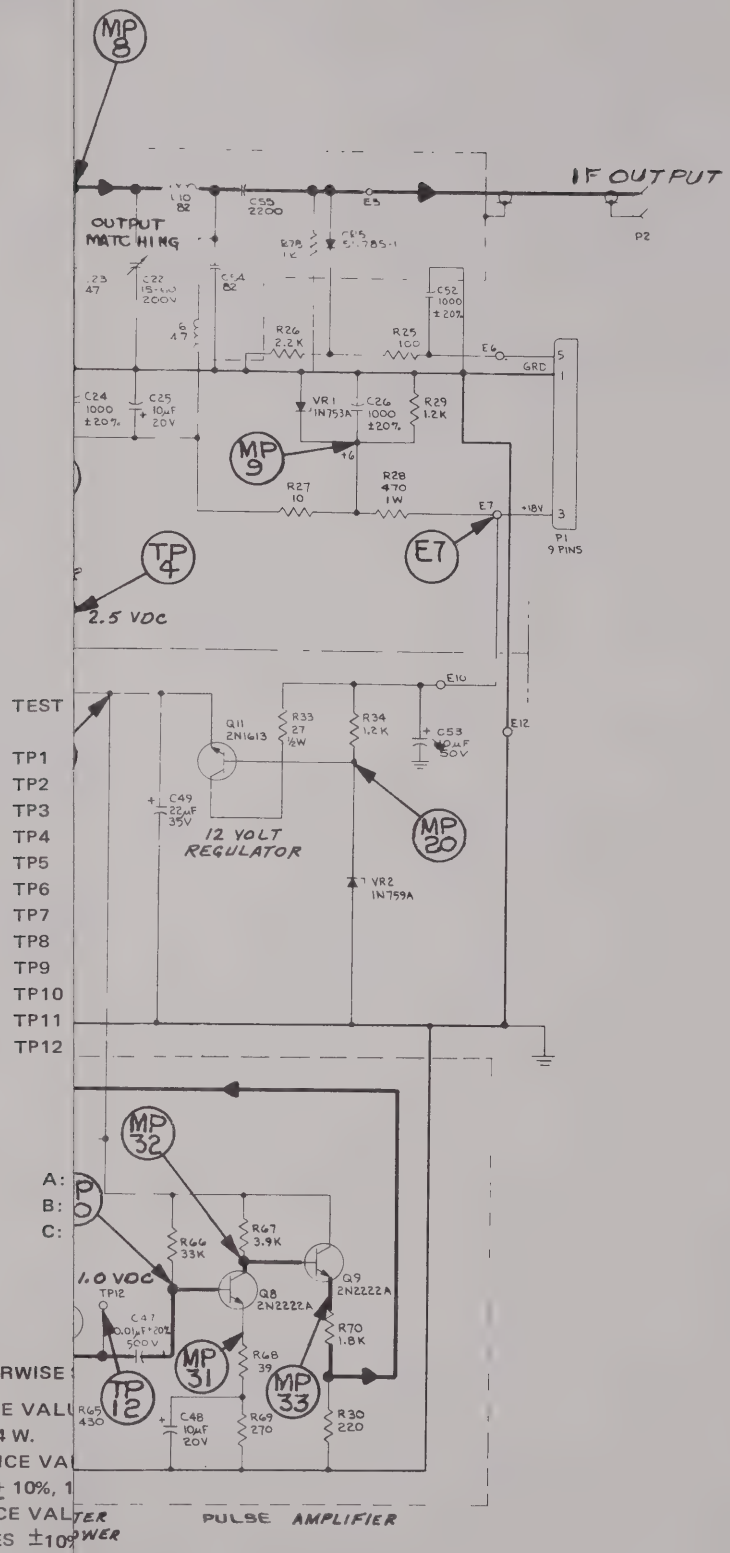


Figure 6-7. Amplifier, Buffer A5, Schematic Diagram



NOTES:

UNLESS OTHERWISE

1. RESISTANCE VALU
OHMS ± 5%, 1/4 W.
2. CAPACITANCE VA
PICOFARADS ± 10%, 1
3. INDUCTANCE VAL
MICROHENRIES ±10
4. ALL VOLTAGE ME
TAKEN WITH A HIGH
ANCE METER (HP427

Electrical Noise Limiter A5, Schematic Diagram

TEST POINT VOLTAGES

TP1	
TP2	12 V ± 1 V
TP3	10 V ± 2 V
TP4	2.5 V ± 0.5 V
TP5	0
TP6	1.5 V ± 0.5 V
TP7	2 V ± 0.5 V
TP8	1 V ± 0.2 V
TP9	10 V ± 2 V
TP10	11 V ± 1 V
TP11	5 V ± 0.2 V
TP12	1 V ± 0.2 V

Z3
A: PULSE DETECTOR
B: AGC CONTROL
C: PULSE AMPLIFIER

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS ± 5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN PICOFARADS ± 10%, 1000V.
3. INDUCTANCE VALUES ARE IN MICROHENRIES ±10%.
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

Figure 6-8. Electrical Noise Limiter A5, Schematic Diagram

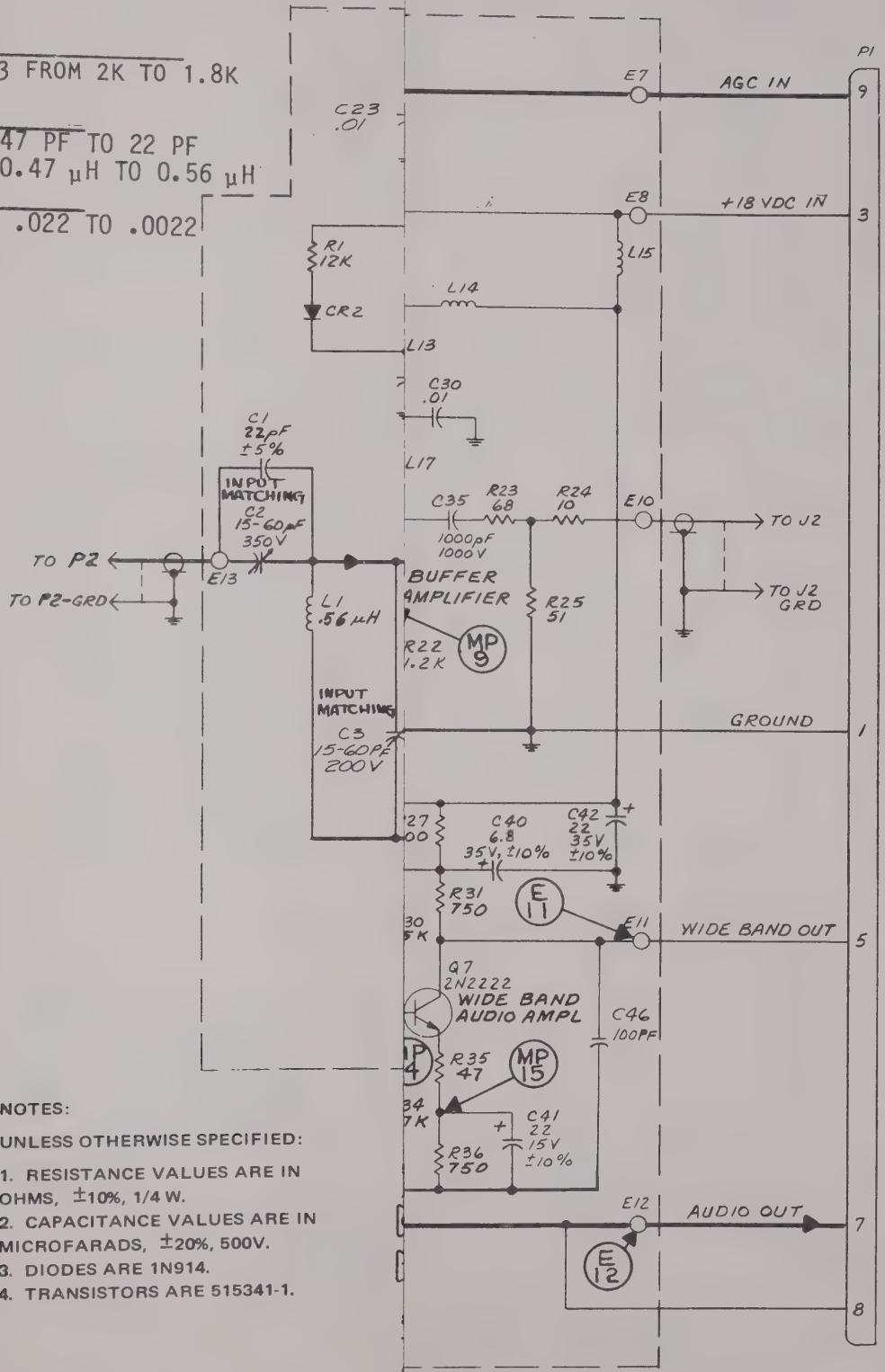
CONFIGU

R30 FROM 16K TO 7.5K
R31 FROM 4.7K TO 750 OHMS
R34 FROM 2.2K TO 2.7K
R35 FROM 82 to 47 OHMS
R36 FROM 1K TO 750 OHMS

R3 FROM 2K TO 1.8K

C1 FROM 47 PF TO 22 PF
L1 FROM 0.47 µH TO 0.56 µH

C43 FROM .022 TO .0022



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±10%, 1/4 W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 515341-1.

te Frequency Amplifier A6, Schematic Diagram

Changed - August, 1980

CONFIGURATION CHANGES

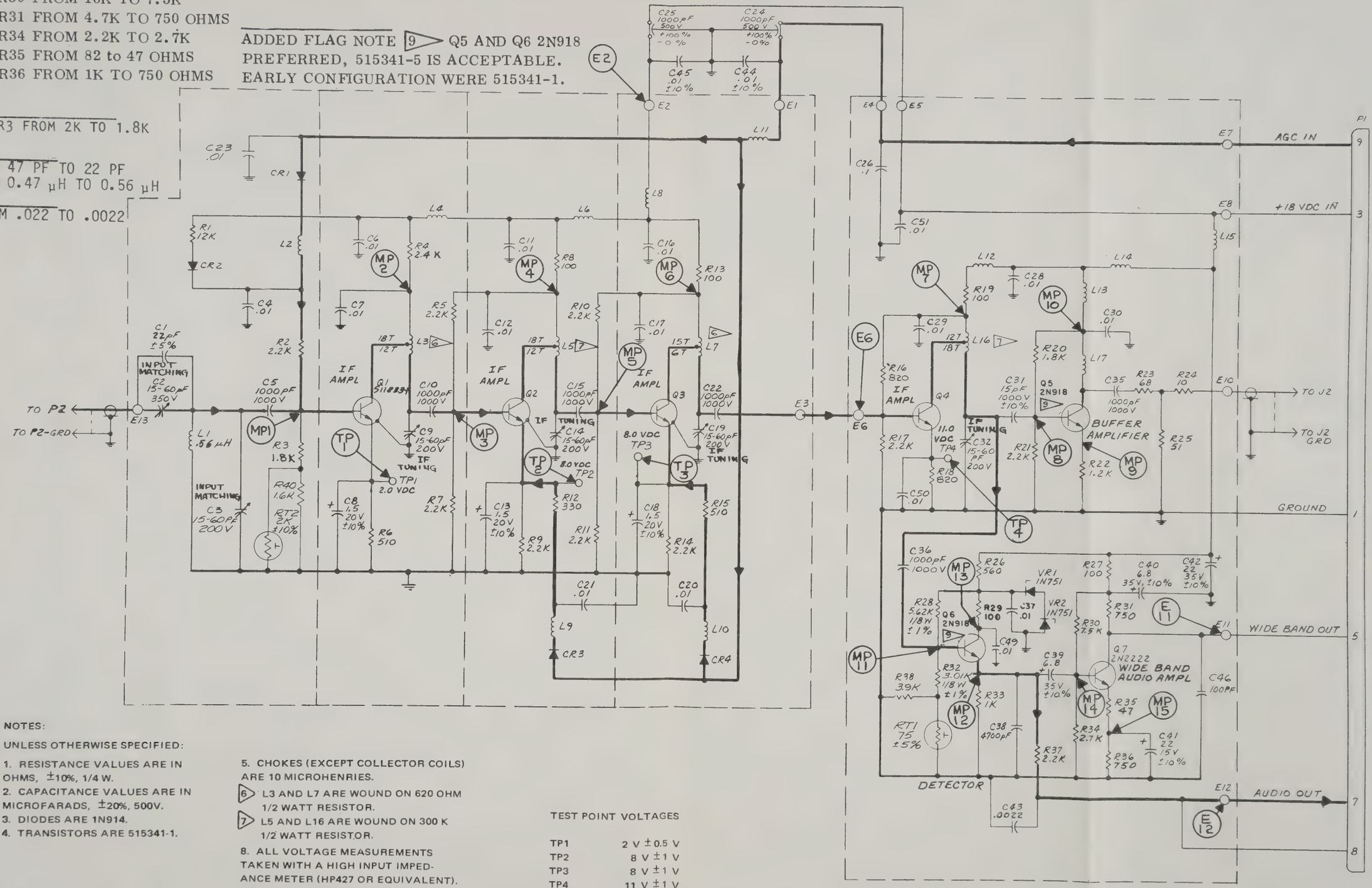
R30 FROM 16K TO 7.5K
R31 FROM 4.7K TO 750 OHMS
R34 FROM 2.2K TO 2.7K
R35 FROM 82 to 47 OHMS
R36 FROM 1K TO 750 OHMS

ADDED FLAG NOTE 9 Q5 AND Q6 2N918 PREFERRED, 515341-5 IS ACCEPTABLE. EARLY CONFIGURATION WERE 515341-1.

R3 FROM 2K TO 1.8K

C1 FROM 47 PF TO 22 PF
L1 FROM 0.47 µH TO 0.56 µH

C43 FROM .022 TO .0022



NOTES:

UNLESS OTHERWISE SPECIFIED:

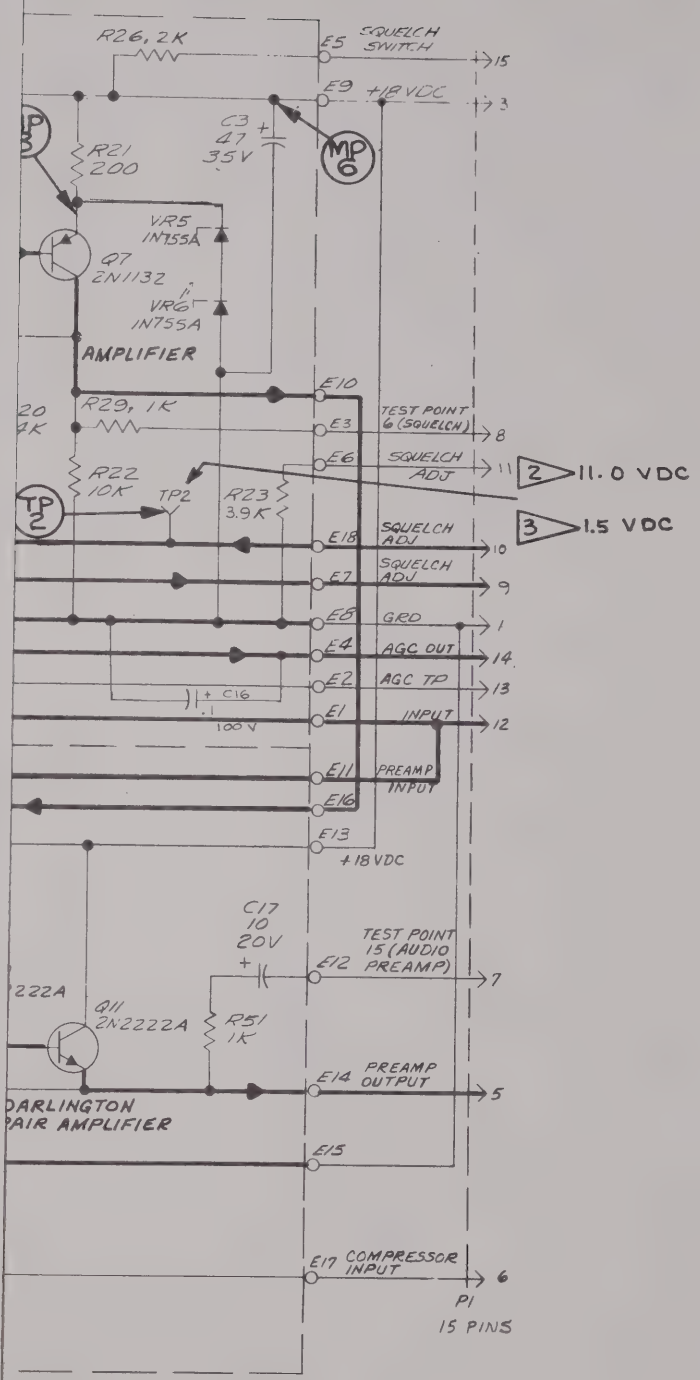
1. RESISTANCE VALUES ARE IN OHMS, ±10%, 1/4 W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 515341-1.
5. CHOKES (EXCEPT COLLECTOR COILS) ARE 10 MICROHENRIES.
6. L3 AND L7 ARE WOUND ON 620 OHM 1/2 WATT RESISTOR.
7. L5 AND L16 ARE WOUND ON 300 K 1/2 WATT RESISTOR.
8. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).
9. PART NUMBER 515341-5 IS ACCEPTABLE IN THIS LOCATION.

TEST POINT VOLTAGES

TP1	2 V ±0.5 V
TP2	8 V ±1 V
TP3	8 V ±1 V
TP4	11 V ±1 V

Figure 6-9. Intermediate Frequency Amplifier A6, Schematic Diagram

Changed - August, 1980



TEST POINT VOLTAGES

TP1	12 V ± 1 V
TP2	11 V ± 1 V
TP3	3 V ± 0.5 V
TP4	4.5 V ± 0.5 V
TP5	4 V ± 0.5 V
TP6	6 V ± 1 V
	2 V ± 0.5 V
TP7	5 V ± 0.5 V
TP8	2 V ± 0.5 V
	1 V ± 0.3 V
TP9	6.5 V ± 0.5 V
TP10	8 V ± 1 V
TP11	15 V ± 1.5 V
TP12	18 V $^{+0.6\ V}_{-2\ V}$

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. NO SIGNAL INPUT.
2. RECEIVER UNSQUELCHED.
3. RECEIVER SQUELCHED.
4. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
5. CAPACITANCE VALUES ARE IN MICROFARADS, ± 10%.
6. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

N CHANGES

) 1.2K

AF/AGC Squelch A3, Schematic Diagram

y Configuration) (P/N 8004239G1)

Changed - August, 1980

TEST POINT VOLTAGES

TP1	12 V ± 1 V
TP2	11 V ± 1 V
TP3	3 V ± 0.5 V
TP4	4.5 V ± 0.5 V
TP5	4 V ± 0.5 V
TP6	6 V ± 1 V
	2 V ± 0.5 V
TP7	5 V ± 0.5 V
TP8	2 V ± 0.5 V
	1 V ± 0.3 V
TP9	6.5 V ± 0.5 V
TP10	8 V ± 1 V
TP11	15 V ± 1.5 V
TP12	18 V $^{+0.6}_{-2}$ V

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. NO SIGNAL INPUT.
2. RECEIVER UNSQUELCHED.
3. RECEIVER SQUELCHED.
4. RESISTANCE VALUES ARE IN OHMS, ± 5%, 1/4 W.
5. CAPACITANCE VALUES ARE IN MICROFARADS, ± 10%.
6. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

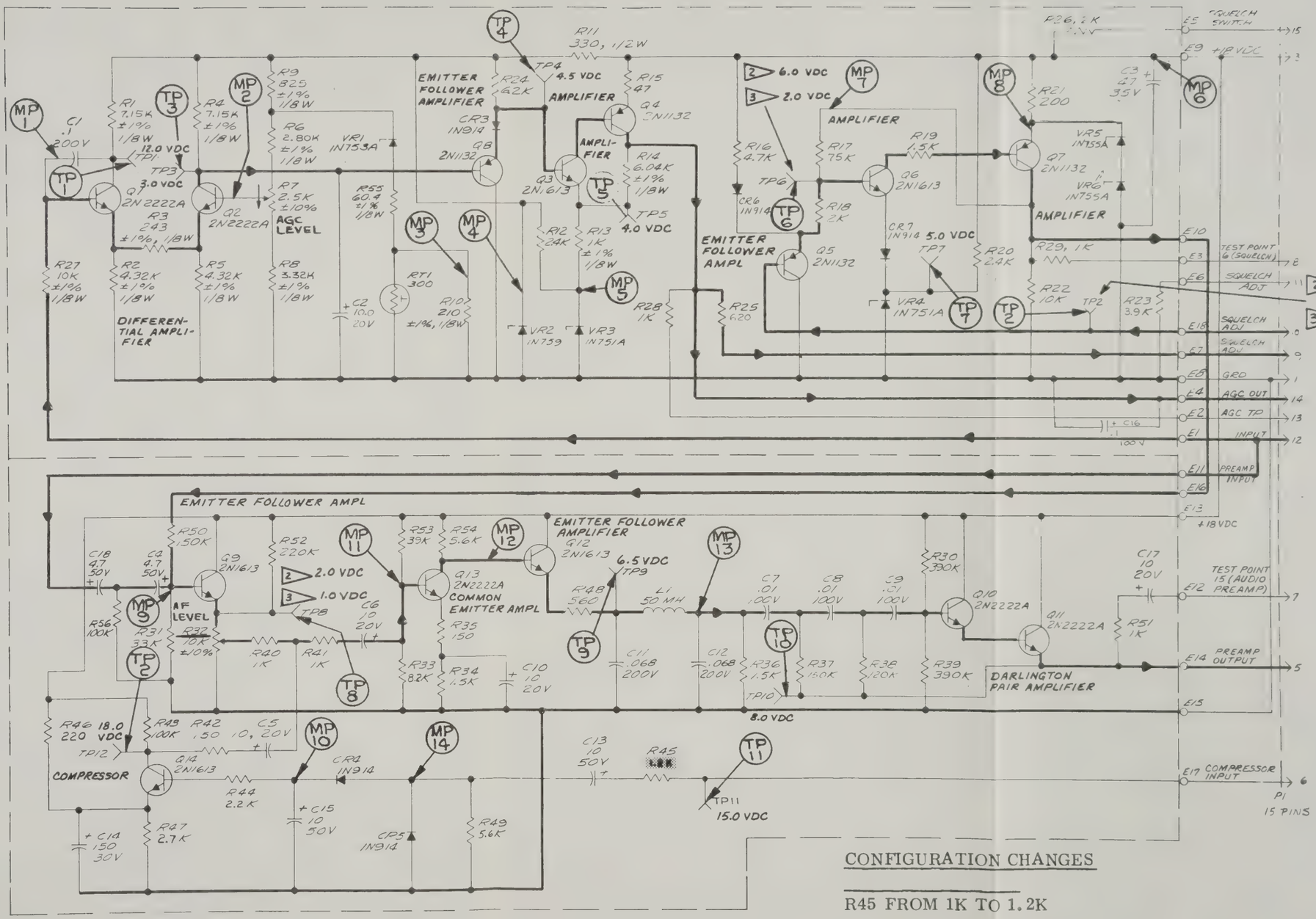
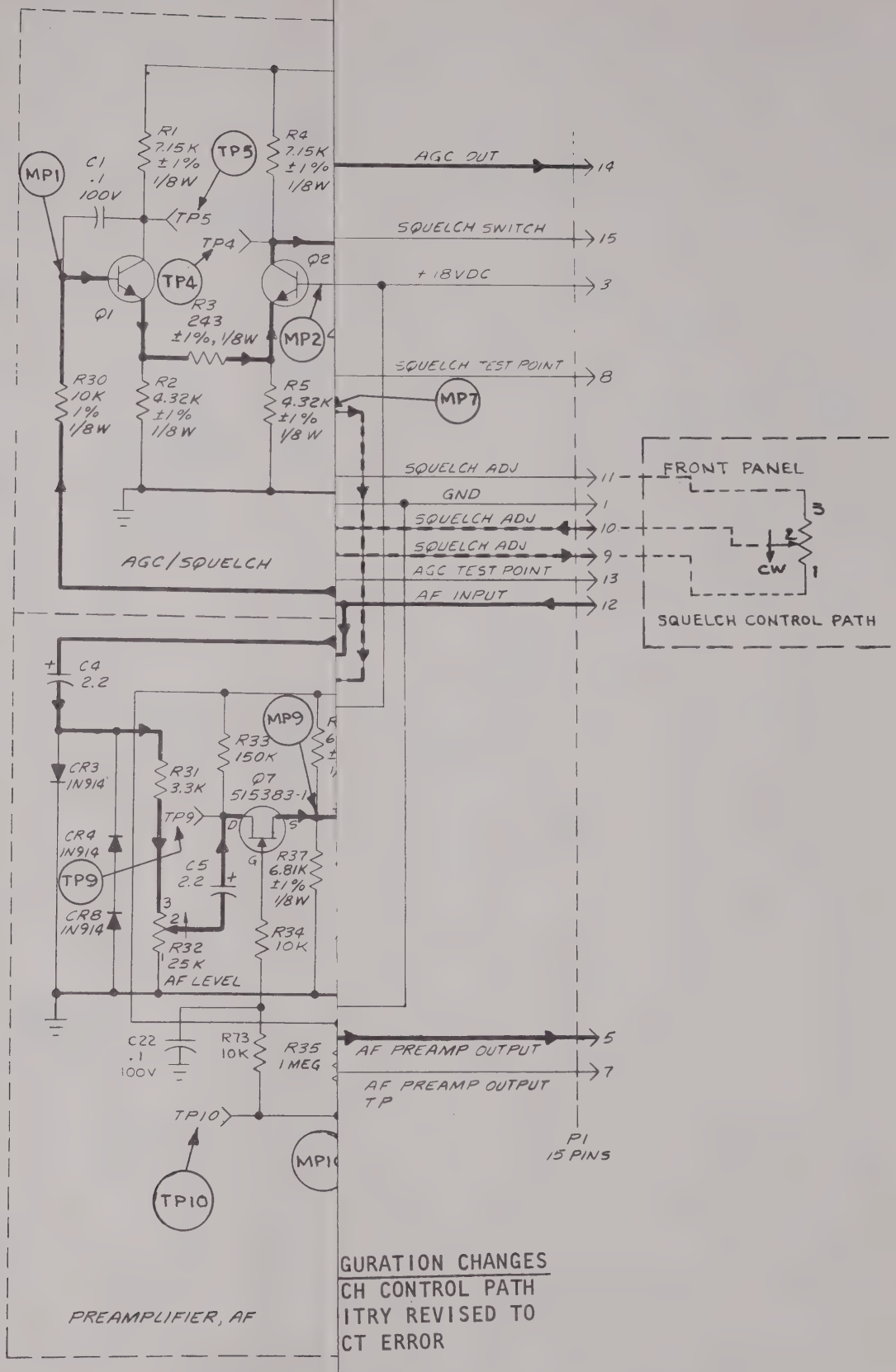


Figure 6-10. Preamplifier AF/AGC Squelch A3, Schematic Diagram (Early Configuration) (P/N 8004239G1)

Changed - August, 1980

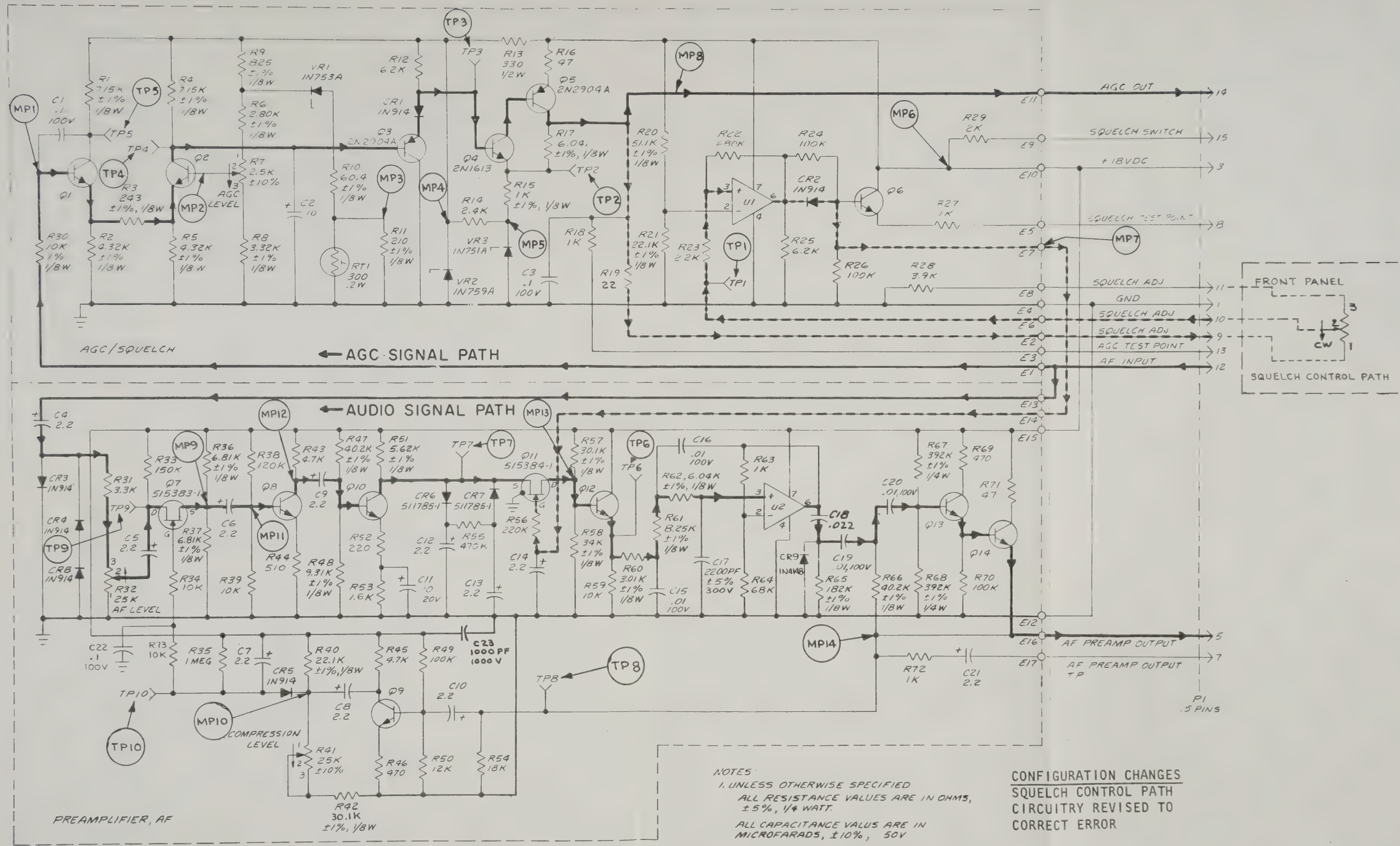


GURATION CHANGES
CH CONTROL PATH
ITRY REVISED TO
CT ERROR

ROM 0.01 TO 0.022

, AF/AGC Squelch A3, Schematic Diagram
1) (Later Configuration)

Changed - August, 1980



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT.
   ALL CAPACITANCE VALUS ARE IN MICROFARADS, ±10%, 50V
   ALL TRANSISTOR 2N2222A
2. U1 & U2 PART NO. 511854-1

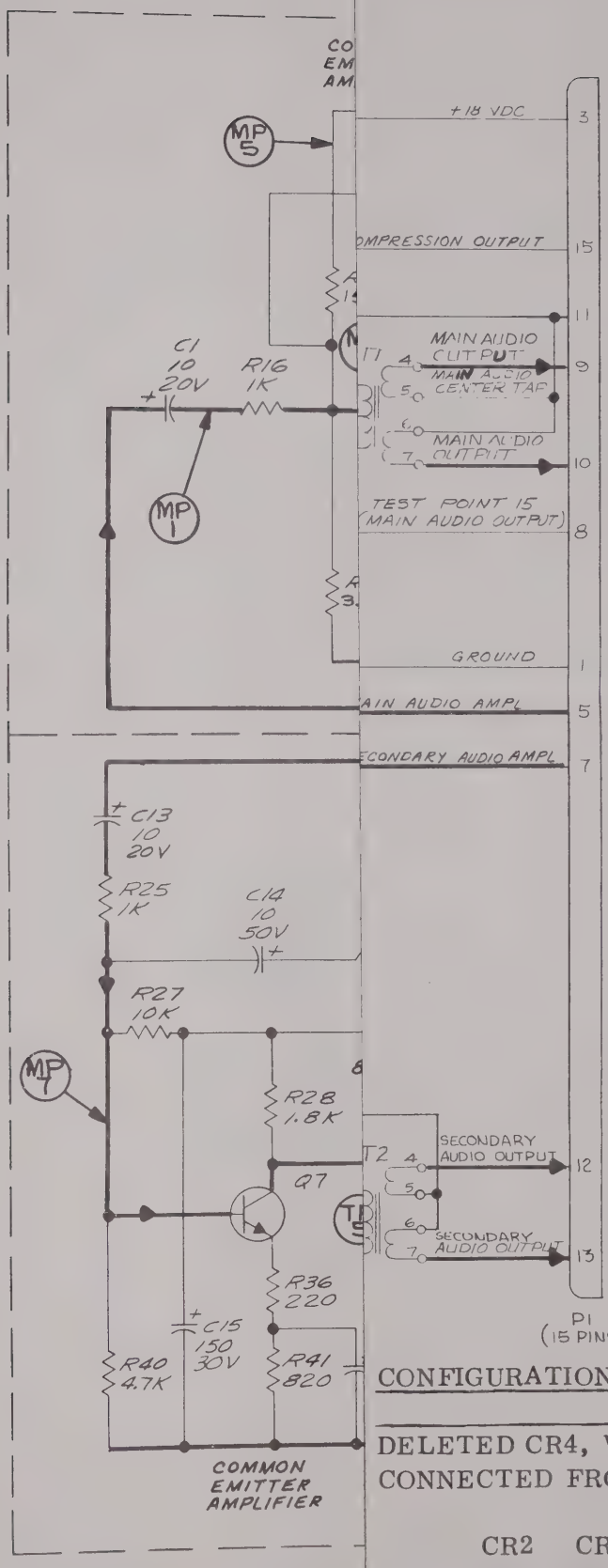
CONFIGURATION CHANGES

SQUELCH CONTROL PATH CIRCUITRY REVISED TO CORRECT ERROR

C18 FROM 0.01 TO 0.022

Figure 6-10A. Preamplifier, AF/AGC Squelch A3, Schematic Diagram (8008586G1) (Later Configuration)

Changed - August, 1980



TEST POINT VOLTAGES

TP1	1.0 V ±0.3 V
TP2	7.5 V ±0.5 V
TP3	1 V ±0.3 V
TP4	1 V ±0.2 V
TP5	8.5 V ±1 V
TP6	1 V ±0.2 V

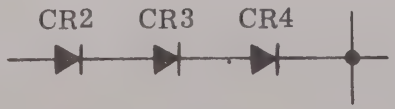
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 2N1613.
5. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

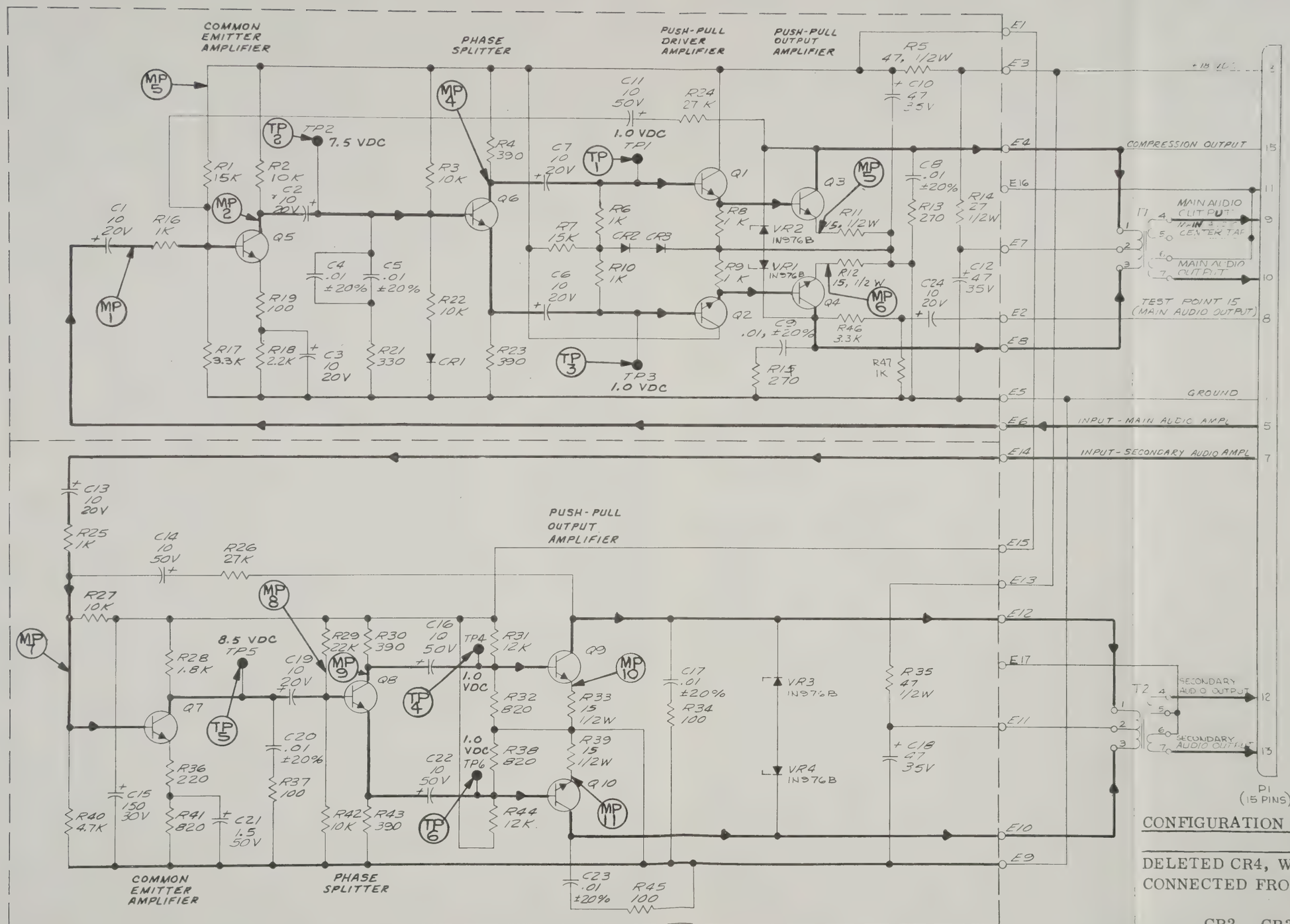
CONFIGURATION CHANGES

DELETED CR4, WAS ORIGINALLY CONNECTED FROM CR3 TO R8, R9



quency Amplifier A4, Schematic Diagram

Changed - August, 1980



TEST POINT VOLTAGES

TP1	1.0 V ± 0.3 V
TP2	7.5 V ± 0.5 V
TP3	1 V ± 0.3 V
TP4	1 V ± 0.2 V
TP5	8.5 V ± 1 V
TP6	1 V ± 0.2 V

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 500V.
3. DIODES ARE 1N914.
4. TRANSISTORS ARE 2N1613.
5. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

CONFIGURATION CHANGES

DELETED CR4, WAS ORIGINALLY CONNECTED FROM CR3 TO R8, R9

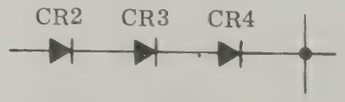
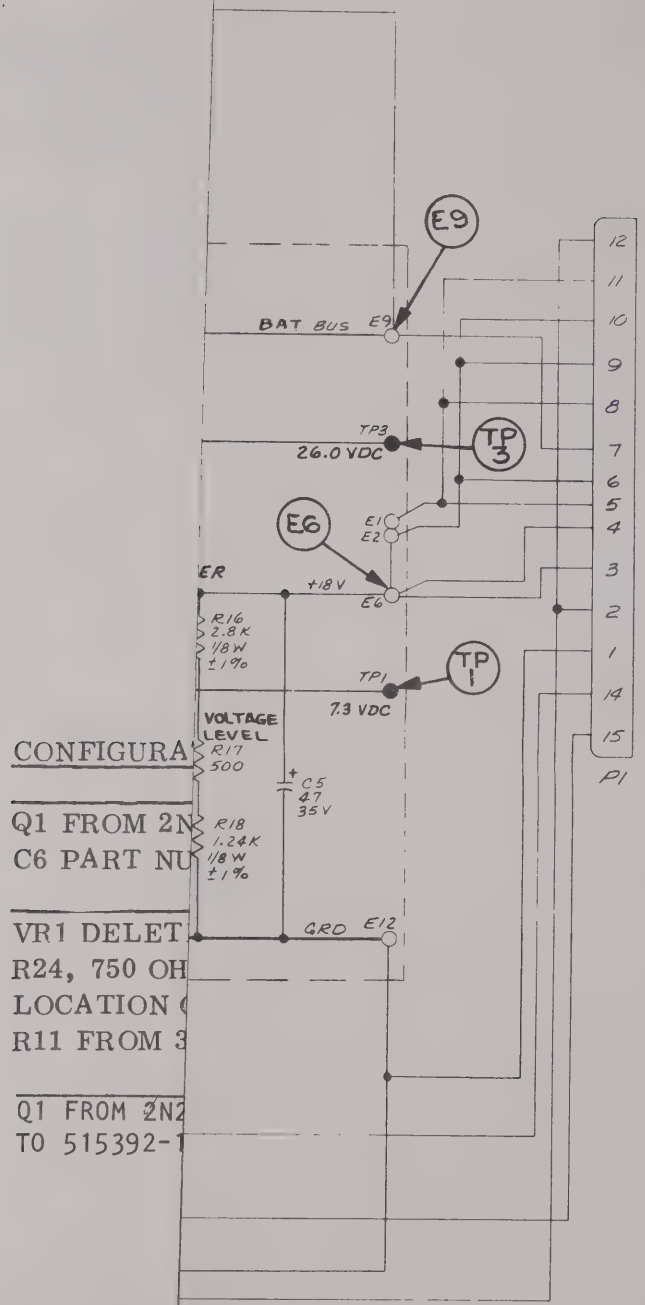


Figure 6-11. Audio Frequency Amplifier A4, Schematic Diagram



6-12. Power Supply PS1, Schematic Diagram

Changed - August, 1980

TEST POINT VOLTAGES

TP1	7.3 V ±1 V
TP2	27 V ±3 V
TP3	26 V ±3 V
TP4	27 V ±3 V
TP5	<0.5 V 30 V ±3 V
TP6	26 V ±3 V

CONFIGURATION CHANGES

OVER CURRENT SENSOR

Q1 FROM 2N1132 TO 2N2904A
C6 PART NUMBER CHANGE ONLY.

OVER CURRENT LOCKOUT

VR1 DELETED
R24, 750 OHM ADDED AT SAME LOCATION OF VR1
R11 FROM 3.3K TO 1.3K

Q1 FROM 2N2904A
TO 515392-1

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. JUMPER STRAPS SHOWN IN POSITION FOR 120V OPERATION.
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/4 W.
3. CAPACITANCE VALUES ARE IN MICROFARADS. ±10%
4. ALL VOLTAGE MEASUREMENTS TAKEN WITH A HIGH INPUT IMPEDANCE METER (HP427 OR EQUIVALENT).

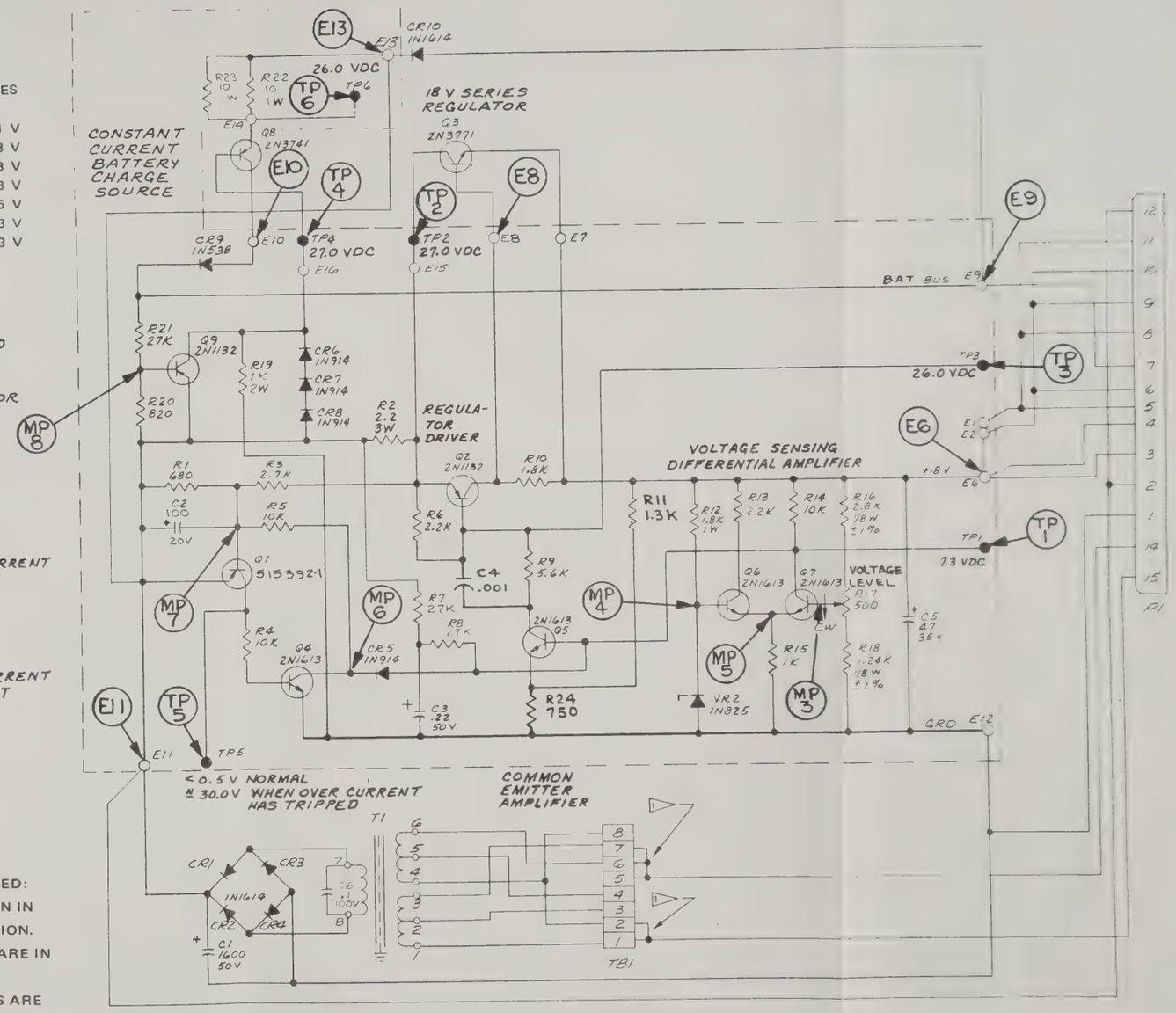
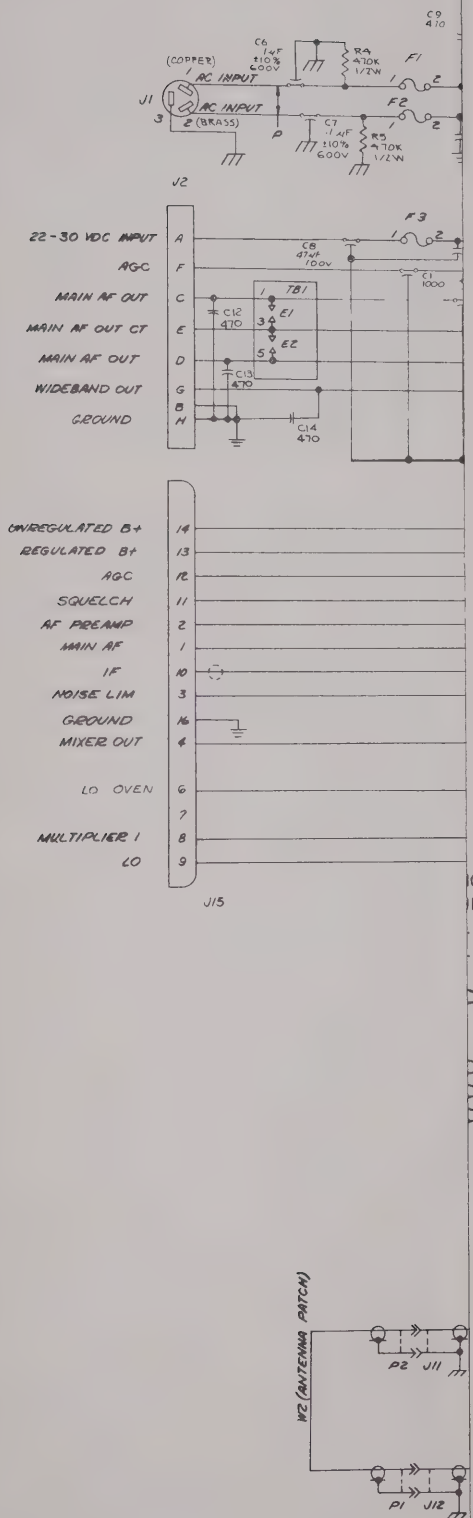


Figure 6-12. Power Supply PS1, Schematic Diagram



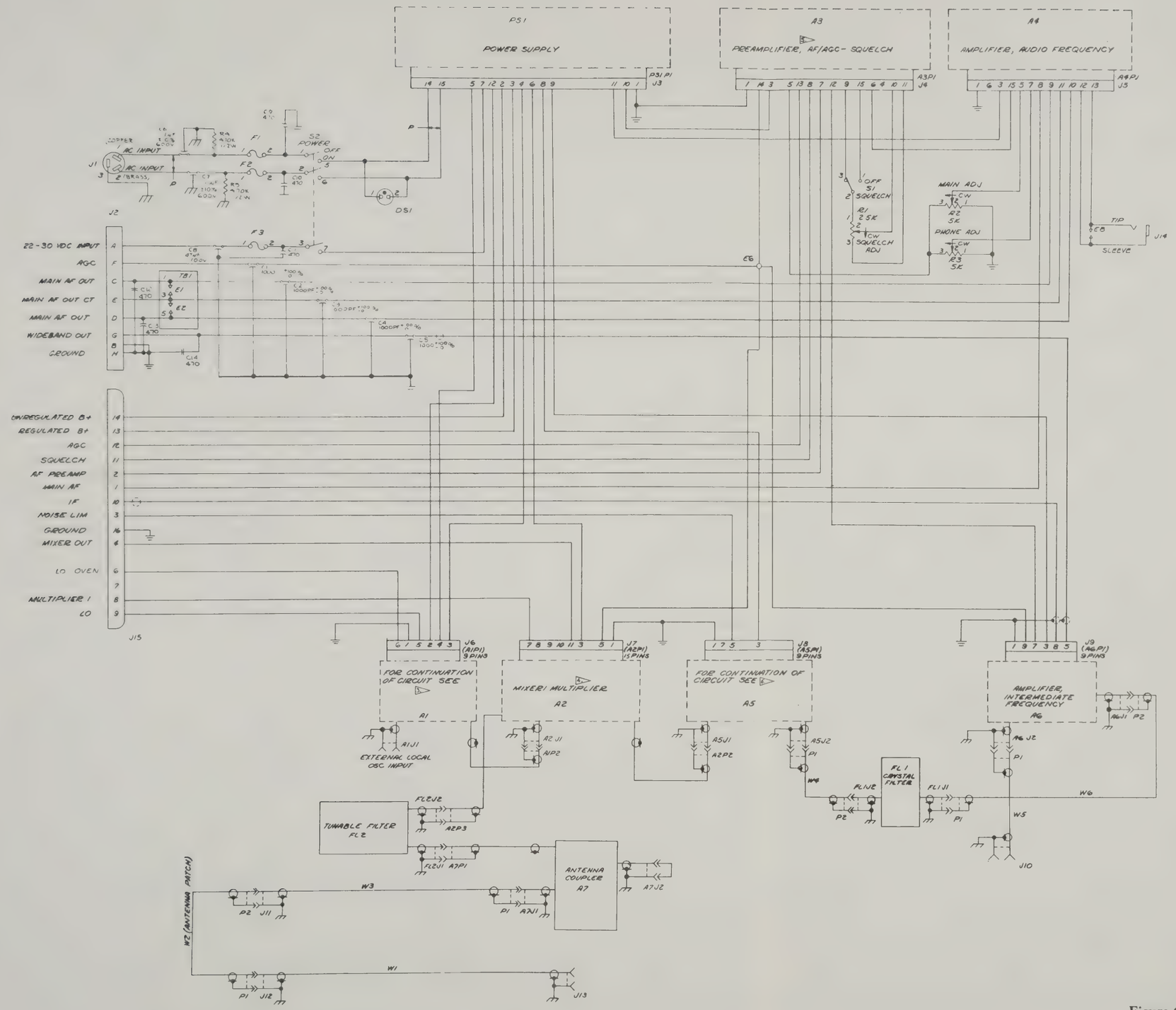
CONFIGURATION CHANGES

NOTES 3 THRU 6 ADDED

R4 AND R5 ADDED
"BRASS" AND "COPPER" REVERSED

OTES:
NLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, ½ W.
ALL CAPACITANCE VALUES ARE IN PICOFARADS, ±10%, 500 V.
FOR CRYSTAL OSCILLATOR SEE FIGURES 6-1, 6-2, AND 6-2A.
FOR SYNTHESIZER SEE FIGURE 6-15.
FOR OSCILLATOR MULTIPLIER SEE FIGURE 6-2C.
FOR VHF MIXER/MULTIPLIER SEE FIGURES 6-3 AND 6-4.
FOR PREAMPLIFIER, AF/AGC SQUELCH SEE FIGURES 6-10 AND 6-10A.
FOR BUFFER AMPLIFIER SEE FIGURE 6-7.
FOR ELECTRICAL NOISE LIMITER SEE FIGURE 6-8.

F Receiver, Schematic Diagram



CONFIGURATION CHANGES

NOTES 3 THRU 6 ADDED

R4 AND R5 ADDED
"BRASS" AND "COPPER" REVERSED

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, ½ W.
2. ALL CAPACITANCE VALUES ARE IN PICOFARADS, ±10%, 500 V.

A1 FOR CRYSTAL OSCILLATOR SEE FIGURES 6-1, 6-2, AND 6-2A.
FOR SYNTHESIZER SEE FIGURE 6-15.
FOR OSCILLATOR MULTIPLIER SEE FIGURE 6-2C.

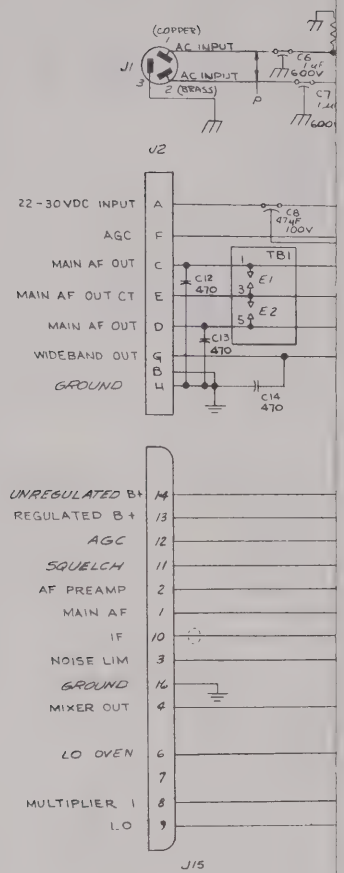
A2 FOR VHF MIXER/MULTIPLIER SEE FIGURES 6-3 AND 6-4.

A3 FOR PREAMPLIFIER, AF/AGC SQUELCH SEE FIGURES 6-10 AND 6-10A.

A5 FOR BUFFER AMPLIFIER SEE FIGURE 6-7.

A6 FOR ELECTRICAL NOISE LIMITER SEE FIGURE 6-8.

Figure 6-13. VHF Receiver, Schematic Diagram



CONFIGURATION CHANGES

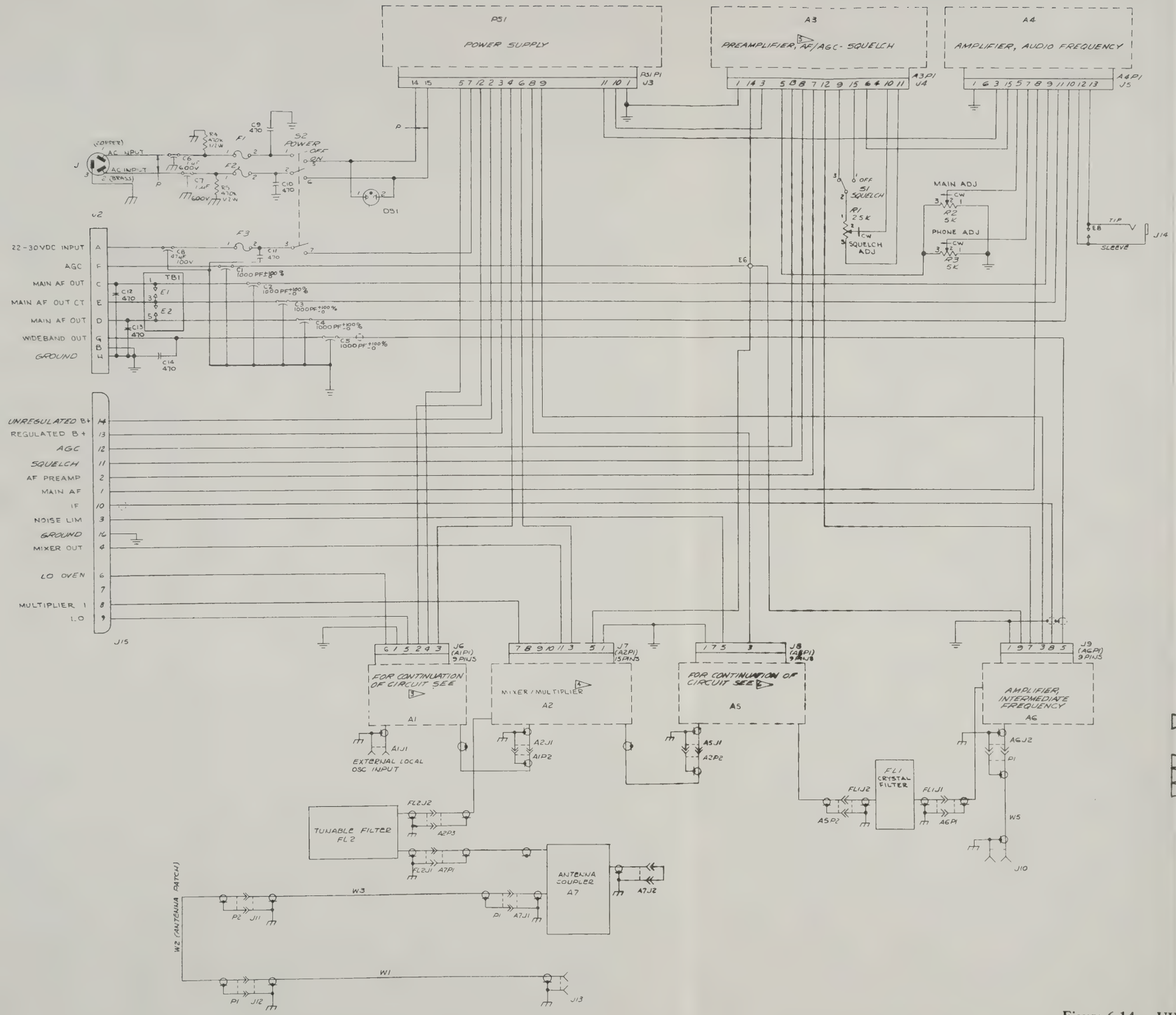
NOTES 3 THRU 6 ADDED

R4 AND R5 ADDED
"BRASS" AND "COPPER" REVERSED

NOTES:
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, ½ W.
2. ALL CAPACITANCE VALUES ARE IN PICOFARADS, ±10%, 500 V.
3. FOR CRYSTAL OSCILLATOR SEE FIGURES 6-1, 6-2, AND 6-2A.
   FOR SYNTHESIZER SEE FIGURE 6-15.
   FOR OSCILLATOR MULTIPLIER SEE FIGURE 6-2C.
4. FOR UHF MIXER/MULTIPLIER SEE FIGURES 6-5 AND 6-6.
5. FOR PREAMPLIFIER, AF/AGC SQUELCH SEE FIGURES 6-10 AND 6-10A.
6. FOR BUFFER AMPLIFIER SEE FIGURE 6-7.
   FOR ELECTRICAL NOISE LIMITER SEE FIGURE 6-8

F Receiver, Schematic Diagram



CONFIGURATION CHANGES

NOTES 3 THRU 6 ADDED

R4 AND R5 ADDED
"BRASS" AND "COPPER" REVERSED

NOTES:
UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS, ± 10%, ½ W.
2. ALL CAPACITANCE VALUES ARE IN PICOFARADS, ±10%, 500 V.
3. FOR CRYSTAL OSCILLATOR SEE FIGURES 6-1, 6-2, AND 6-2A.
   FOR SYNTHESIZER SEE FIGURE 6-15.
   FOR OSCILLATOR MULTIPLIER SEE FIGURE 6-2C.
4. FOR UHF MIXER/MULTIPLIER SEE FIGURES 6-5 AND 6-6.
5. FOR PREAMPLIFIER, AF/AGC SQUELCH SEE FIGURES 6-10 AND 6-10A.
6. FOR BUFFER AMPLIFIER SEE FIGURE 6-7.
   FOR ELECTRICAL NOISE LIMITER SEE FIGURE 6-8

Figure 6-14. UHF Receiver, Schematic Diagram

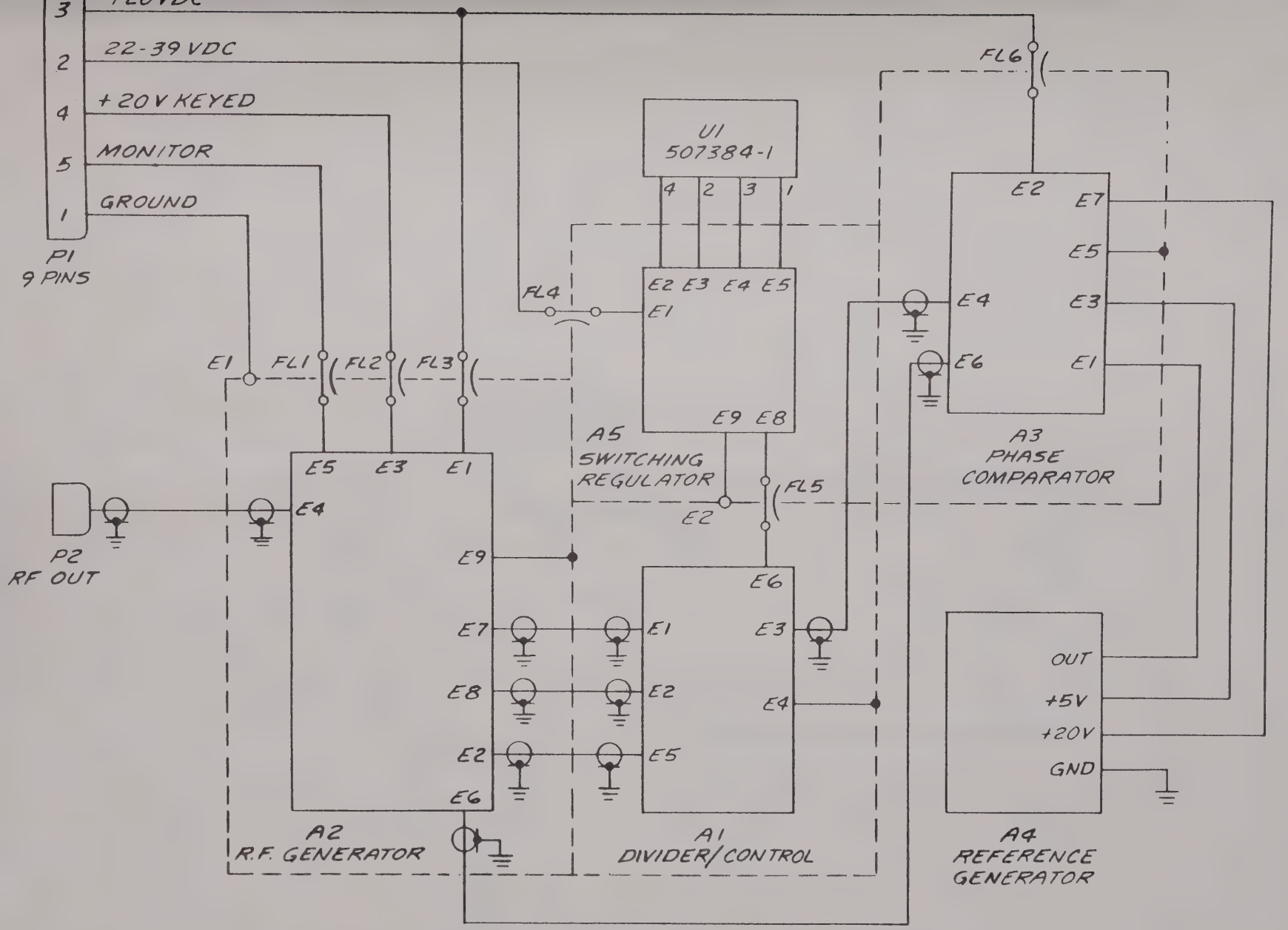
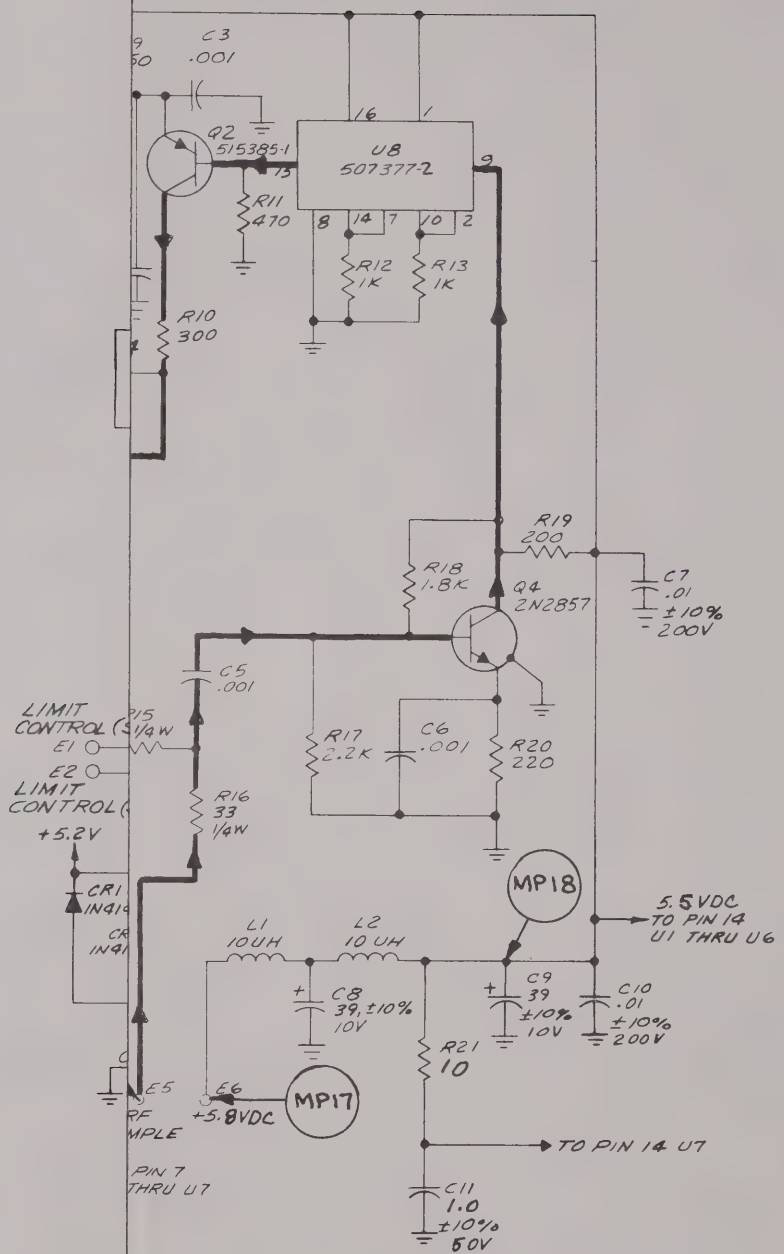
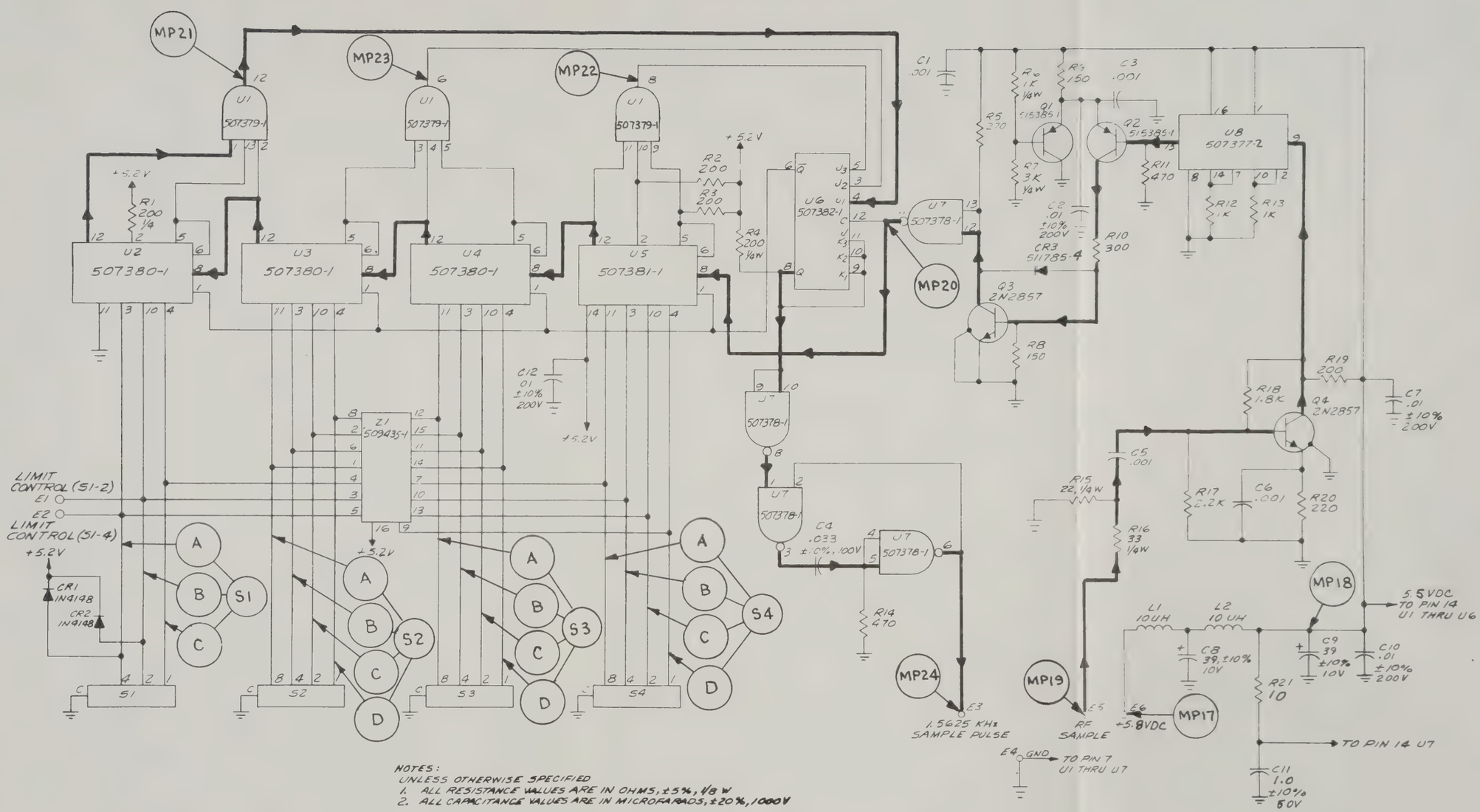


Figure 6-15. Synthesizer A1, Schematic Diagram



ontrol A1A1, Schematic Diagram



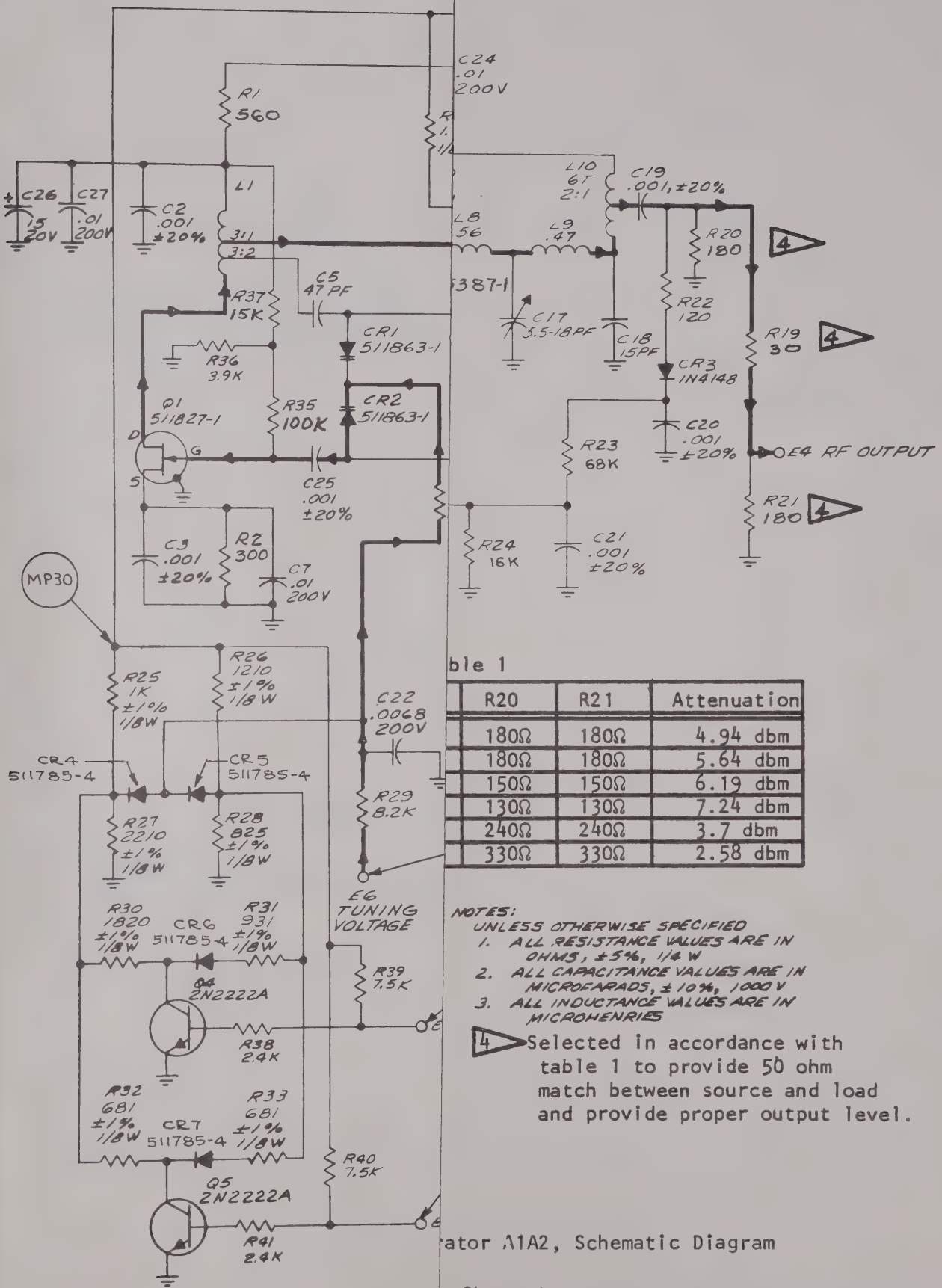
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/8 W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±20%, 1000V

CONFIGURATION CHANGES

CR3 FROM 511785-1 TO 511785-4

R21 WAS 47
C11 WAS 0.01, 200V
VOLTAGE AT E6 WAS 5.5 Vdc

Figure 6-16. Divider/Control A1A1, Schematic Diagram



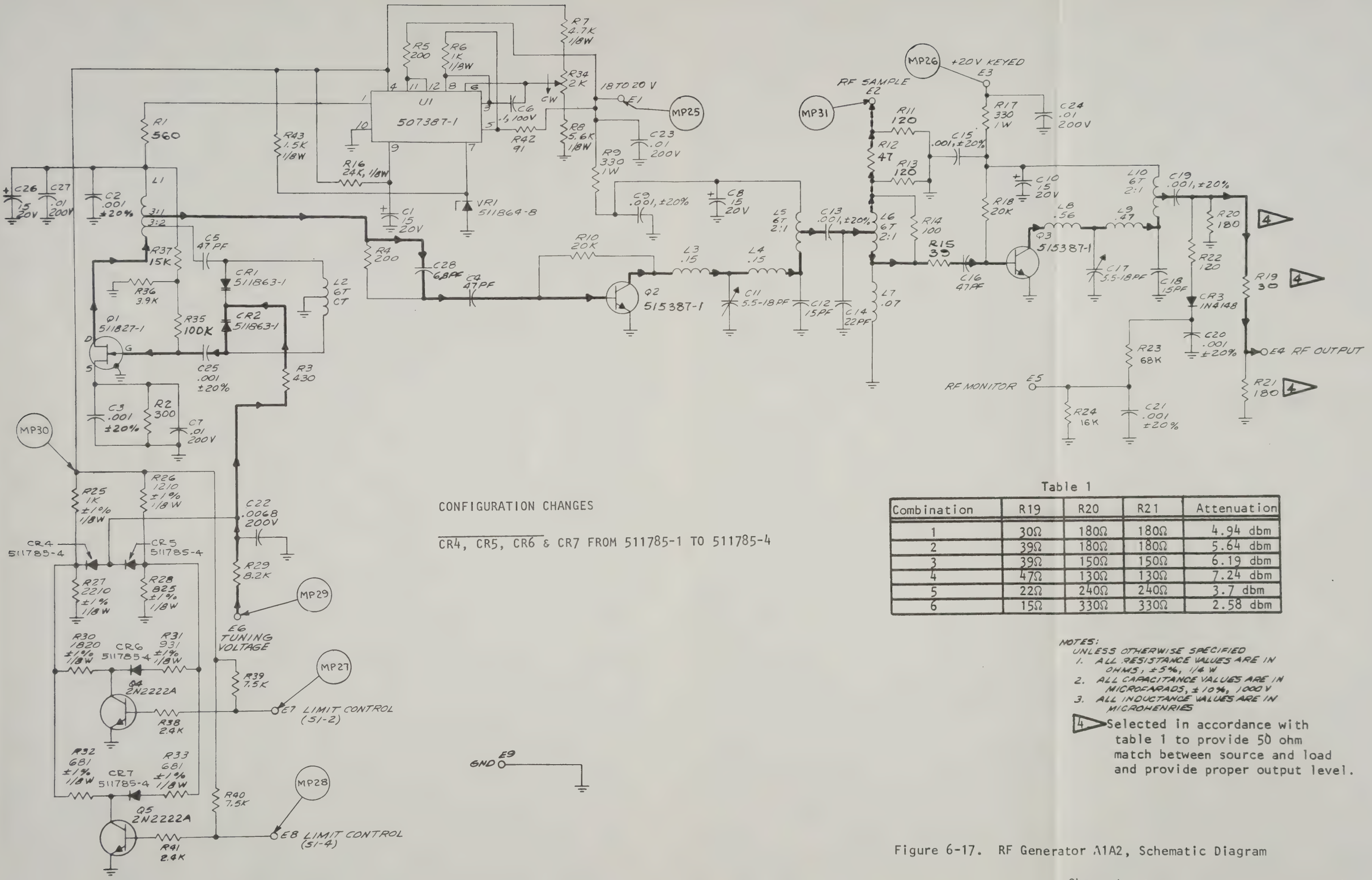
ble 1

	R20	R21	Attenuation
	180Ω	180Ω	4.94 dbm
	180Ω	180Ω	5.64 dbm
	150Ω	150Ω	6.19 dbm
	130Ω	130Ω	7.24 dbm
	240Ω	240Ω	3.7 dbm
	330Ω	330Ω	2.58 dbm

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 1000 V
3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES

4 Selected in accordance with table 1 to provide 50 ohm match between source and load and provide proper output level.

ator A1A2, Schematic Diagram



CONFIGURATION CHANGES

CR4, CR5, CR6 & CR7 FROM 511785-1 TO 511785-4

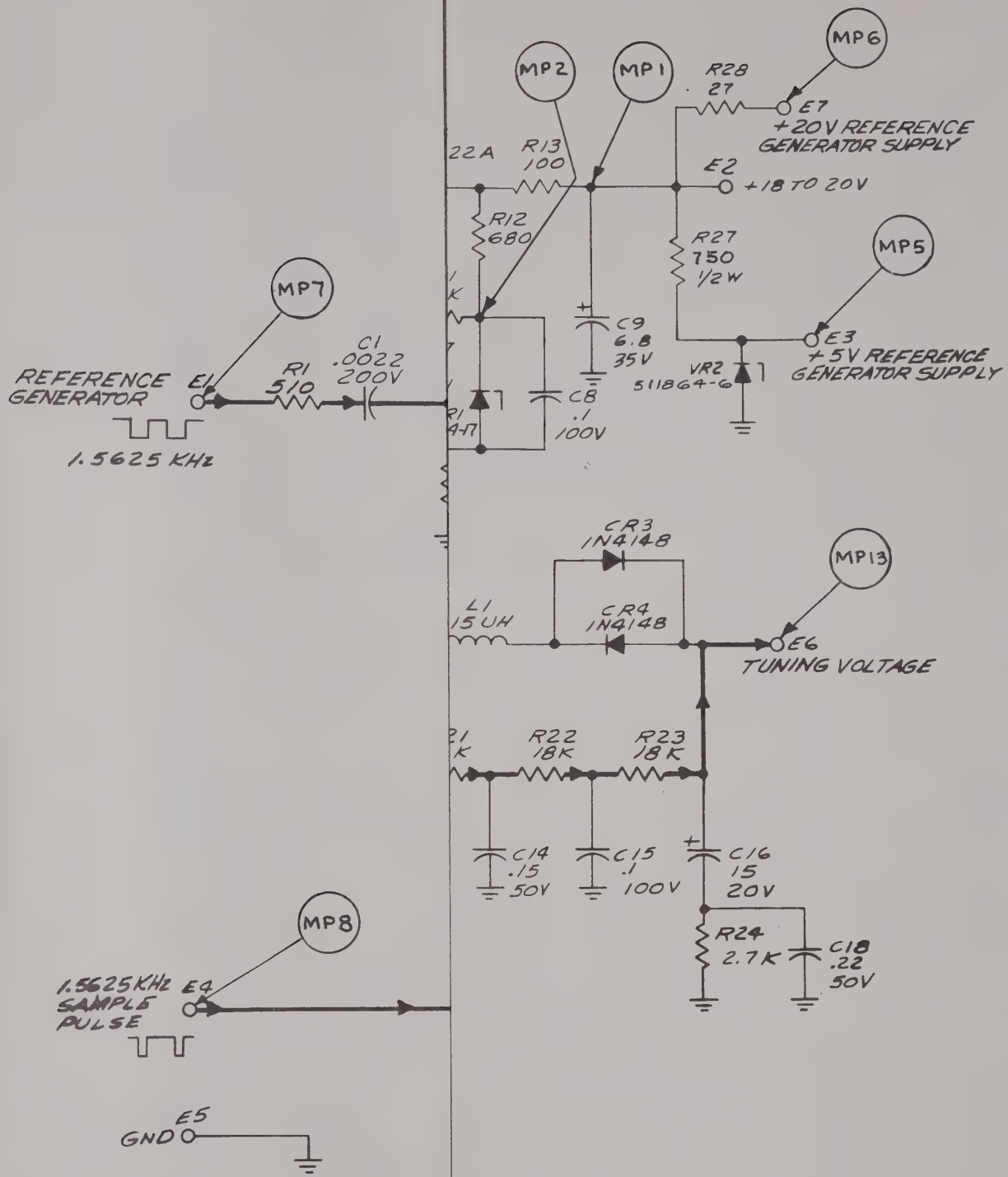
Table 1

Combination	R19	R20	R21	Attenuation
1	30Ω	180Ω	180Ω	4.94 dbm
2	39Ω	180Ω	180Ω	5.64 dbm
3	39Ω	150Ω	150Ω	6.19 dbm
4	47Ω	130Ω	130Ω	7.24 dbm
5	22Ω	240Ω	240Ω	3.7 dbm
6	15Ω	330Ω	330Ω	2.58 dbm

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 1000 V
3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES

4 Selected in accordance with table 1 to provide 50 ohm match between source and load and provide proper output level.

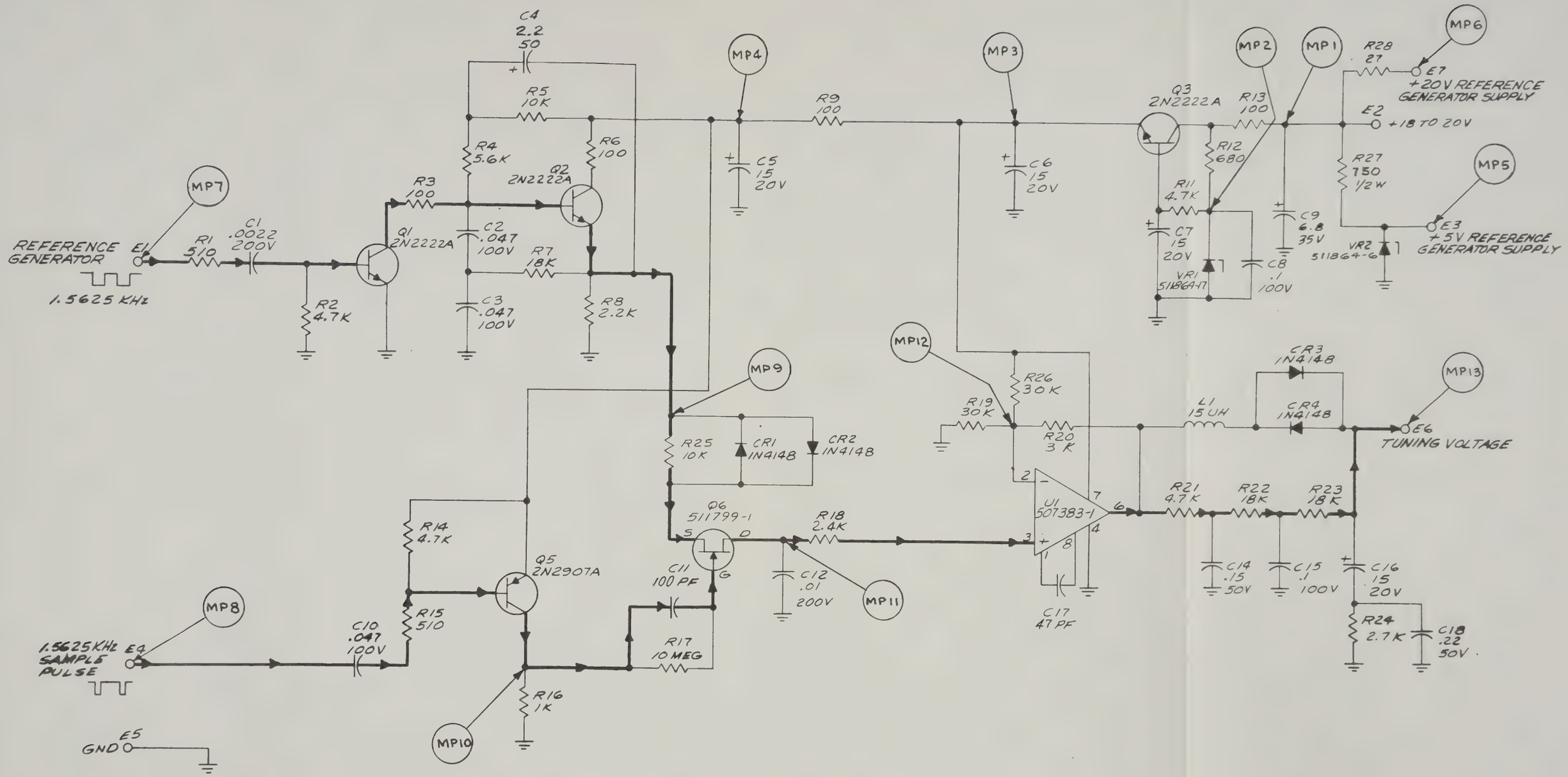
Figure 6-17. RF Generator A1A2, Schematic Diagram



THERWISE SPECIFIED
RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W
CAPACITANCE VALUES ARE IN MICROFARADS,
%, 1000 V

parator A1A3, Schematic Diagram

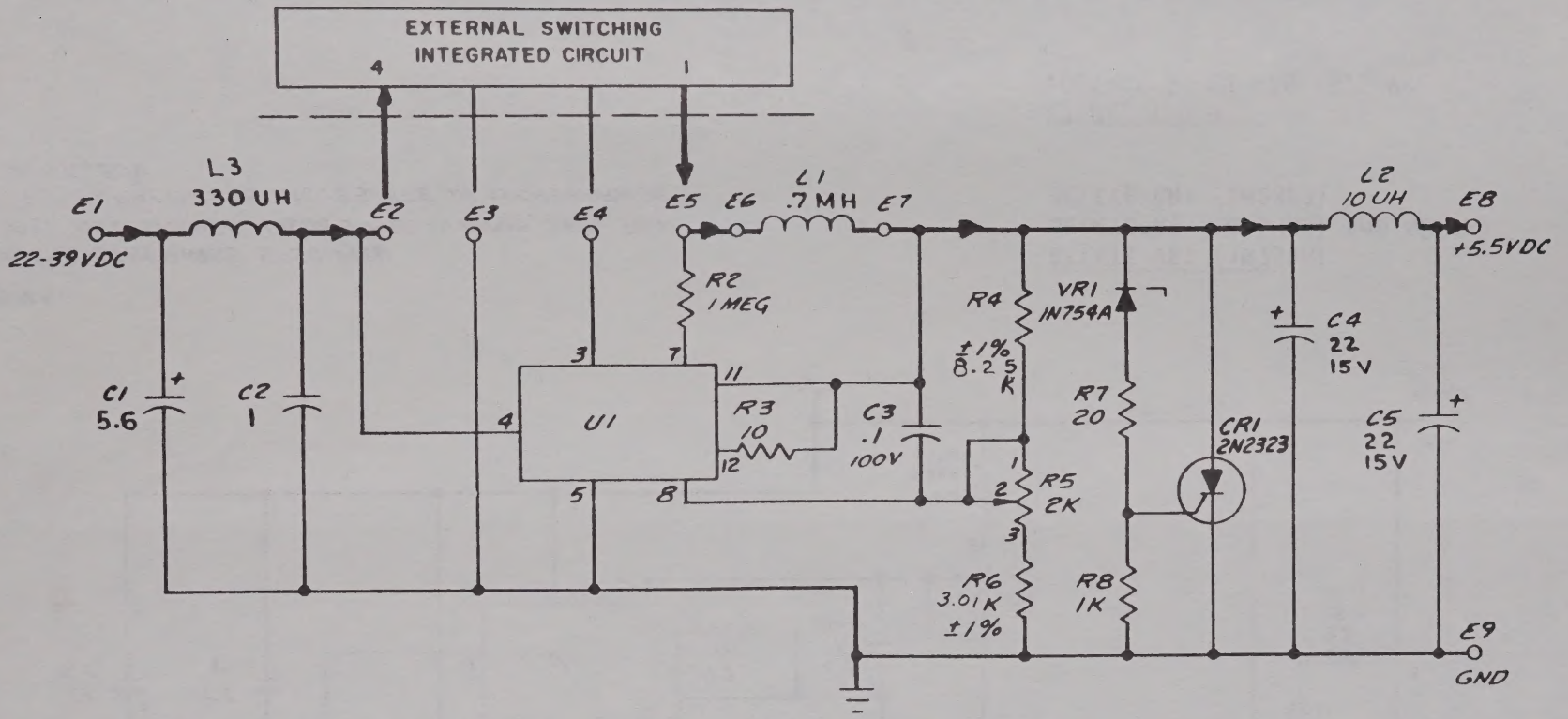
Changed - August, 1980



NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 1000V

Figure 6-18. Phase Comparator A1A3, Schematic Diagram

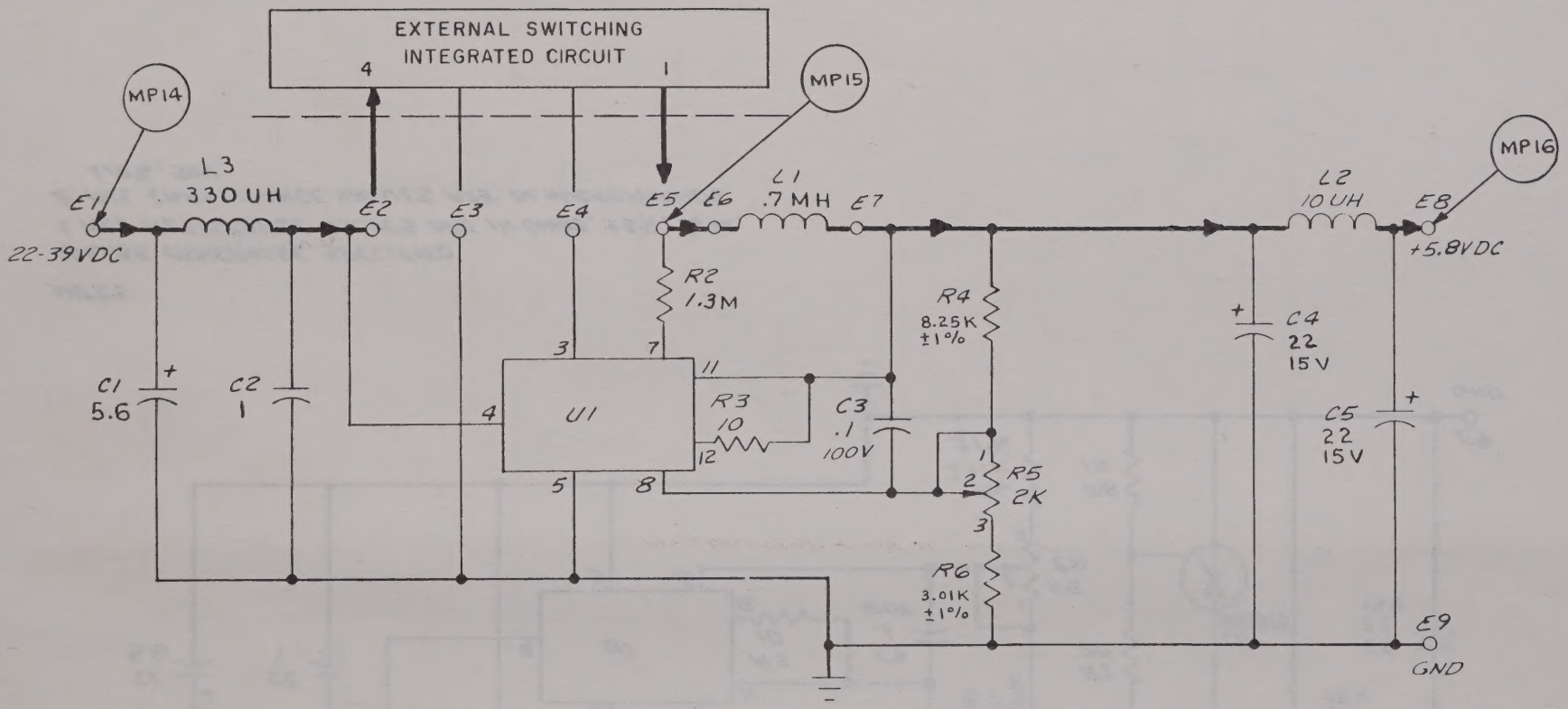


NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ⅛ W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS ±10%, 50V

Figure 6-19. Switching Regulator A1A5 , Schematic Diagram
(Early Configuration)



NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ¼W.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS ±10%, 50V

DELETE VR1 (1N754A)
DELETE R7 (20 OHMS) AND R8(1K)
DELETE CR1 (2N2323)

R2 WAS 1.0 M
VOLTAGE AT E8 WAS +5.5 Vdc

Figure 6-19A. Switching Regulator A1A5, Schematic Diagram (Later Configuration)